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Single electron tunneling of nanoscale $TiSi_2$ islands on Si

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Nanoscale $TiSi_2$ islands are formed by electron beam deposition of a few monolayers of titanium on an atomically clean silicon surface followed by *in situ* annealing at high temperatures (800–1000 °C). The lateral diameter of typical islands are ~5 nm, and they form a nanoscale metal–semiconductor interface. Direct probing of the electrical characteristics of these islands on both *p*- and *n*-type Si substrates was performed using ultrahigh vacuum scanning tunneling microscopy and scanning tunneling spectroscopy. With the vacuum between the tip and the island as a second tunnel junction, we thus form a double-junction system for observation of single electron tunneling (SET) effects. Moreover, the small dimensions of the system allow room temperature observation. The results showed features in the *I–V* spectra attributed to single electron tunneling. Features were more evident when the island–Si junction was in reverse bias. For substrates with a thin epitaxial layer of intrinsic Si, the tunneling related features were enhanced for both doping types. The experimental results are compared with the standard theory and numerical values from the fitting are in agreement with the experimental structures. The results indicate that the nanoscale Schottky barrier of the island–substrate interface can be employed as a tunnel barrier in SET structures.
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I. INTRODUCTION

As the size of electronic devices evolve into the nanometer range, the basic physics of device operation will also evolve from classical behavior to predominantly quantum effects. Among many options considered for nanoelectronics, there has been growing interest in single electronics based on single electron tunneling effects.[1,2]

A nanoscale island ($d<5$ nm) between two tunnel barriers forms a double-barrier structure, which will exhibit these effects. When the energy required to add a single electron to the island becomes much larger than the thermal fluctuation energy, the electron transport is inhibited for a range of voltage. This phenomenon is known as Coulomb blockade.[3] In a double-barrier structure, each tunnel barrier is described as a parallel combination of *R* and *C*, which are then connected in series. With strongly asymmetric junctions ($R_1C_1 \gg R_2C_2$ or vice versa), as the applied bias becomes larger a stepwise increase of current in the current–voltage (*I–V*) relation appears in addition to the Coulomb blockade. This phenomenon is referred to as the Coulomb staircase. The theory of single electron tunneling (SET) is based on the following assumptions.[4] First, a nanoscale island should be small enough that the charging energy of the island e^2/C is much larger than the thermal fluctuation energy kT. For room temperature application, this condition, $e^2/C \gg kT$ requires the capacitance of an island to be in aF range ($a=10^{-18}$). This translates into the size of an island being less than 5 nm. Second, the tunneling resistance R_T of the island should be larger than the quantum of resistance R_K, ~25.8 kΩ, i.e., $R_T \gg R_K$. This requirement comes from the following consideration. The junction is characterized by three time scales: the tunneling time τ_t, the uncertainty time τ_c, and the tunneling event time, τ_r. The tunneling time τ_t is roughly the time spent by the tunneling electron through the barrier ($\sim 10^{-15}$ s). The uncertainty time is associated with the Coulomb energy $\tau_c = R_K C$ ($\sim 10^{-10}$ s). The longest time scale is set by the tunneling resistance and the capacitance: $\tau_r = R_T C$. It is the reciprocal of the tunneling rate event for a junction biased at the Coulomb voltage of e/C. The theory assumes a clear separation of time scales $\tau_t \ll \tau_c \ll \tau_r$. The first inequality states that the tunneling time is negligible while the second one states the requirement of $R_T \gg R_K$, which ensures a reasonably long lifetime of an excess electron on an island before it tunnels out of the island and onto another electrode.[5] The second inequality also implies the classical nature of the number of electrons on the island.

For the SET phenomena to be considered in future device structures, stable operation must be achieved at or near room temperature. Although many nanostructures with double tunnel junctions have demonstrated SET at low temperature,[6–8] only a few reports have successfully shown this effect at room temperature.[9,10] The SET effects were observed in a double-barrier junction structure of tip/gold cluster/self-assembled monolayer of dithiol molecules on a Au substrate.[10] The gold cluster size was found to range between 2 and 5 nm. Other small metal clusters (less than 5 nm) such as gold,[11] silver,[12] or platinum[13] were deposited on an insulator/substrate forming well-established double-barrier junction structures, which showed single electron tunneling effects. Also field evaporation of a tip was used to deposit gold islands on silicon by applying a short pulse between the gold tip and the silicon substrate in a scanning

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tunneling microscope (STM).[14] Much like our study, it was proposed that the tunnel barrier is formed by the Schottky barrier between the metal island and the semiconductor substrate. Room temperature SET results have typically been observed using the spectroscopic function of a STM. In this approach, the separation between the tip and an island is used as one of the tunnel barriers (R_1, C_1) while the island–substrate contact is the other (R_2, C_2). The tip–island distance can be adjusted by changing the tunneling current feedback setpoint, and the I–V characteristics can be measured after freezing the feedback.

Although the prior results demonstrate SET effects, they usually suffer a lack of compatibility with current integrated circuit fabrication technology. For example, an insulating layer made of a polymer may not be suitable for high temperature processes. We have previously introduced approaches to fabricate nanoscale silicide islands[15] and others have examined the detailed structure of $TiSi_2$ islands,[16] but there has been no reported work on single electron charging effects of nanoscale silicide islands. Our previous studies have shown that a thin layer of titanium reacts with the silicon substrate and through annealing leads to the formation of nanometer scale silicide island structures.[17] The phase transition from the metastable C49 phase to the equilibrium C54 phase was not observed in thin films of $TiSi_2$.[18] Another study using STM and transmission electron microscopy (TEM) by Briggs *et al.* confirms the presence of the C49 phase for $TiSi_2$ islands on Si(001) that are incommensurate.[16] Their study indicated that most of the silicide islands were incommensurate C49 $TiSi_2$. A recent study has also explored the surface energies of Ti silicide nanostructures,[19] and supports our previous contentions[20] that the energetics influences the nucleation process. It may be then possible to control the growth mode of silicide islands to achieve the desired nanostructures for single electronics. However, there are still many technical hurdles to overcome to achieve precise control of the island dimensions.

Nonetheless, with our growth processes, it is possible to produce $TiSi_2$ islands that are less than 5 nm in diameter, which is small enough to anticipate that the single electron charging effects will occur at room temperature. Our experiments were performed after forming $TiSi_2$ *in situ* on a Si(111)7×7 surface. The room temperature scanning tunneling spectroscopy I–V results indicate Coulomb blockade and Coulomb staircase on these islands.

II. EXPERIMENT

The main component of the experimental setup is an ultrahigh vacuum (UHV) STM system (Park Scientific, AutoProbe VP) with electron beam deposition, Auger electron spectroscopy (AES), and low energy electron diffraction (LEED). The base pressure of the system was less than 5×10^{-11} Torr. For deposition of the initial films, an *e*-beam evaporator was used with titanium of 99.99% purity. The AES and LEED were obtained using a four-grid rearview LEED optics (Princeton Inst). For AES, the same LEED optics are used as a retarding field analyzer by applying an alternating electric field between the grids and the chassis ground. A load-lock pumped by a turbo pump is used for sample introduction. The whole system rests on an air suspension table for vibration reduction during STM operation.

Various combinations of substrates were used for this study: *n*-type and *p*-type wafers with a doping concentration of $N=10^{17}$ cm^{-3} for either type. Substrates were also studied that were prepared with a thin intrinsic Si layer grown by molecular beam epitaxy (MBE). The Si wafer surfaces were chemically etched and annealed in UHV to 950 °C prior to growth, and the intrinsic Si layer was epitaxially deposited on the atomically clean (*p*- or *n*-type) silicon surfaces at 550 °C. Prior to loading into the UHV STM chamber, all substrates were similarly prepared. The substrate was scribed into rectangles of 0.3 cm×1.5 cm and then fastened onto the sample holder. The sample holder is designed for direct current heating for UHV flashing and annealing. Note that the ambient oxidation and subsequent thermal cleaning of the substrates with the MBE intrinsic layer will reduce the thickness of the intrinsic layer.

After several hours of outgassing at 600 °C (usually overnight), the sample was flashed at 1200 °C for a duration of 30–120 s. Care was taken to keep the chamber pressure below 2×10^{-9} Torr during the flashing. The reconstructed 7×7 surface, confirmed by LEED and STM, was achieved after the heat cleaning. STM revealed that there was no contamination on the surface as several scans of the surface with scan size up to a few microns showed no particular features on the surface other than steps. The clean surface was used as a starting surface for the subsequent titanium deposition.

Titanium was deposited with the substrate at room temperature by electron beam evaporation. The nominal deposition rate used for this study was 0.2 nm/min for thicknesses varying from 1 to 2 monolayers. Following the deposition, the sample was annealed for 30–60 s at temperatures of 800, 900, and 1000 °C. The ramping time from room temperature to the desired temperature was less than 10 s.

STM images obtained right after the annealing show large thermal drift. It usually takes several hours after each annealing before the images show acceptable minimal drift ($\leqslant$1 nm/min) as measured from successive images. The STM images were obtained in the constant current mode with a tunneling current between 0.5 and 1 nA, and a bias varying from −2 to 2 V. After identifying an appropriate island, I–V spectroscopy was obtained on the island with the feedback loop frozen. For each I–V spectra, the signals were averaged from 5 to 10 times. Since it was suggested that oscillation of the system could lead to artificial current oscillation,[21] I–V data were also obtained with different ramping rates to distinguish artifacts from real effects. We have occasionally observed similar oscillation artifacts,[21] and these scans were discarded. The typical voltage range for the I–V measurements was from −3 to 3 V. The I–V data were numerically differentiated to display dI/dV spectra.

III. RESULTS

In $TiSi_2$ formation, there is a transition from the metastable C49 phase to the stable C54 phase upon annealing. However, when the thickness of the film is less than 25 nm,

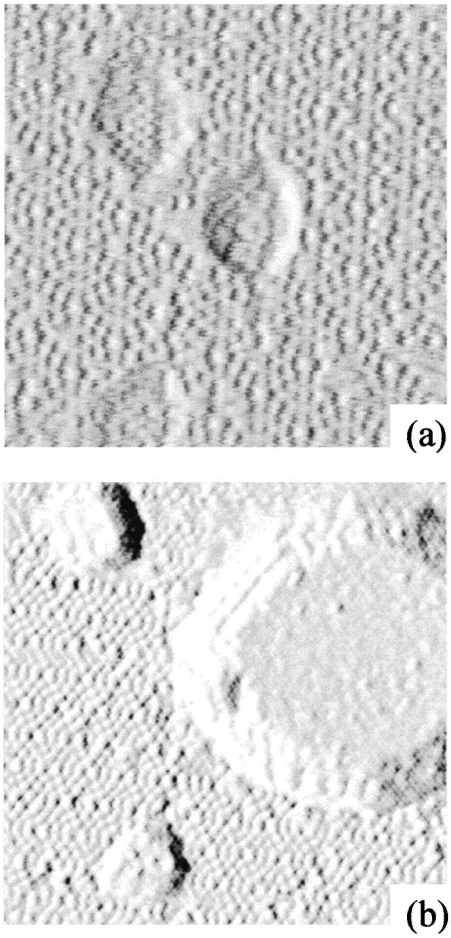

FIG. 1. STM images of $TiSi_2$ islands on a Si(111) surface after 0.2 nm Ti deposition: (a) after annealing at 800 °C, scan size is 30×30 nm^2 and (b) After annealing at 900 °C, scan size is $\sim40\times40$ nm^2.

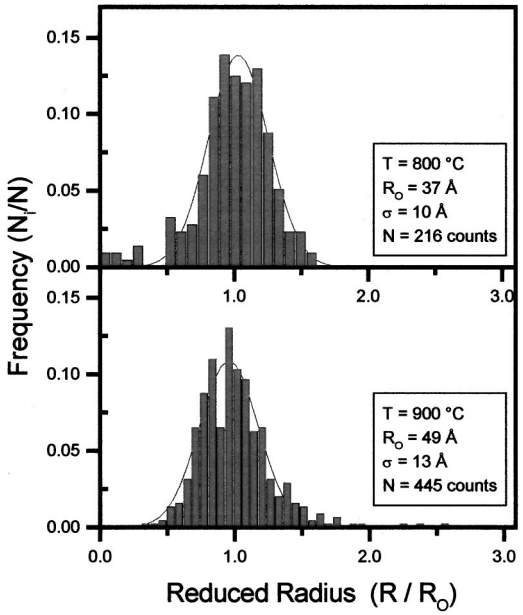

FIG. 2. Size distribution of $TiSi_2$ islands on the Si(111) surfaces shown in Fig. 1. The distribution was obtained by analysis of STM images with scan size of 0.5×0.5 μm^2.

the resulting $TiSi_2$ island phase is C49, and the transition from the C49 to the C54 phase is not observed.[18] Thus, it is assumed that for the thin titanium layer in our experiments, the islands are the C49 phase. A recent study using STM and TEM by Briggs *et al.* confirms the presence of the C49 phase of $TiSi_2$ for incommensurate islands on Si(001).[16]

Shown in Fig. 1 are STM images of $TiSi_2$ islands obtained after 0.1 nm Ti deposition and annealing at 800 and 900 °C, respectively. After annealing at 900 °C, the average island size increases from that of 800 °C due to island coalescence and/or Ostwald ripening.[17,22] The size distributions are presented in Fig. 2.

In Figs. 3(a) and 3(b), we show I–V spectra for $TiSi_2$ islands with ~5 nm in diameter, which display features characteristic of SET effects. The I–V curves were obtained with various ramping rates, and when the SET related effects were observed the curves were independent of ramping rate. We show results from islands with either an *n*- or *p*-type substrate. For the *n*-type substrate, the conductance peak is more obvious for positive sample bias, while for the *p*-type substrates, the conductance peak is present for negative sample bias. The differences in the magnitude of the current is most likely attributed to slightly different tip–sample distances. In Figs. 4(a) and 4(b), we show I–V and dI/dV curves obtained from an island formed on a substrate with a Si epilayer. The intrinsic Si layer was epitaxially deposited on atomically clean (*p*- or *n*-type) silicon surfaces before titanium deposition and subsequent annealing take place in the STM cham-

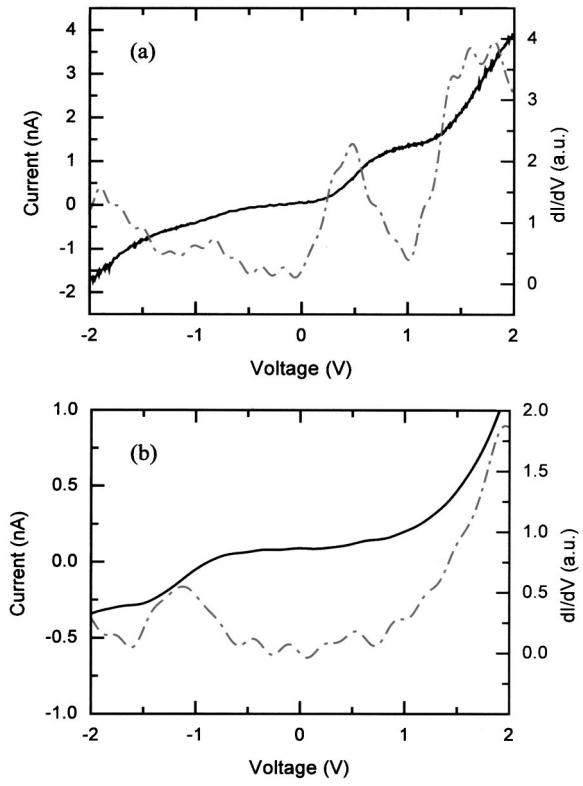

FIG. 3. I–V and dI/dV spectra obtained from: (a) an island on an *n*-type substrate and (b) an island on a *p*-type substrate. The I–V curves were numerically differentiated to obtain the dI/dV traces.

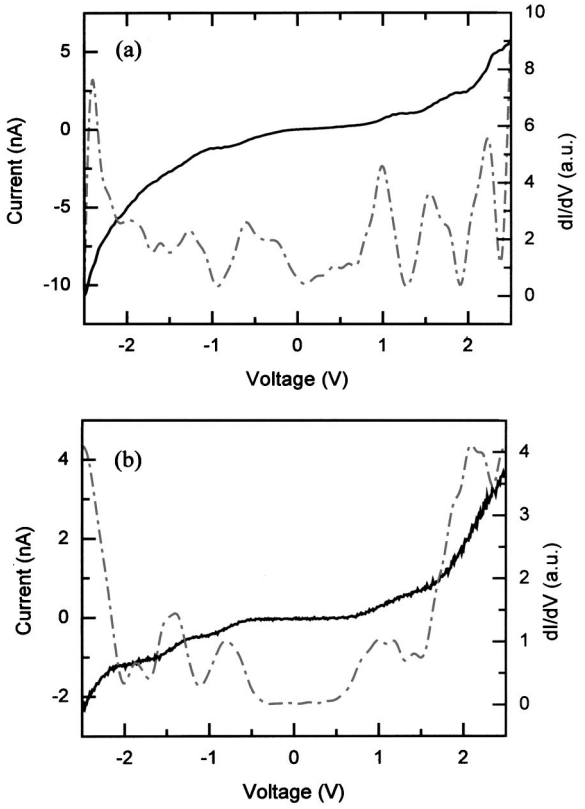

FIG. 4. I–V and dI/dV spectra obtained from: (a) an island on an n-type substrate with a 3 nm intrinsic Si buffer layer and (b) an island on a p-type substrate with a 5 nm buffer layer.

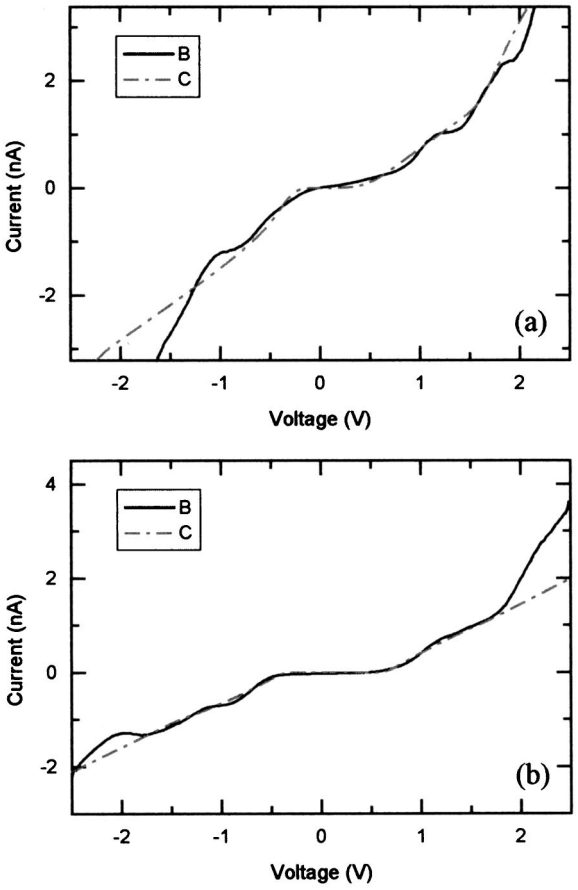

FIG. 5. Experimental I–V results (from Fig. 4) and a least square fit from the model show good agreement at low voltage but deviate from each other at higher voltage.

ber. For this case, a series of steps in the I–V curves are clearly observed in both polarities for either p- or n-type substrates.

Using the double-barrier junction model,[4] least square fits of the I–V results were obtained as shown in Fig. 5. Overall, the Coulomb blockade behavior is well reproduced from the model fit, while it failed to show the higher voltage current steps. In the following sections, we will discuss the significance of the silicide–silicon interface as a tunnel barrier, and the dependence of the SET on the extra layer of intrinsic silicon.

IV. DISCUSSION

A. On nanoscale m-s tunnel barrier

Our results indicate that SET effects of Coulomb blockade and Coulomb staircase are observed in the tip–metallic island–semiconductor double-barrier junction structures. These phenomena were observed in substrates with both doping types. The general trend is that the conductance peaks are more obvious when the metal–semiconductor interface is reverse biased regardless of the type of the substrate.

Most previous studies of SET at room temperature have employed an insulator as a tunnel barrier between the metallic island and the semiconducting substrate[12,13] while the STM forms the second tunnel junction. In a prior study, silver nanoparticles were deposited on an Sb-passivated silicon surface and SET effects were displayed at room temperature.[12] A small silver island that is located near densely populated islands showed SET while the densely populated islands showed metallic behavior. The authors claimed that SET may be due to the lateral tunneling barrier between the islands rather than the tunneling through the barrier formed at the metal–semiconductor interface.[21] Contrary to the above study in the case of silver particles on silicon, our STM images show that $TiSi_2$ islands are well separated from each other. Hence, lateral tunneling is not expected to play a significant role in our case. The prior study of field evaporated gold nanoislands on H-terminated, p-type Si(111) showed distinct features up to 4 V bias, which is well beyond the voltage range where we observed oscillations.[14] Here also, the authors suggested lateral diffusion to surroundings may account for the observations.

The phenomenon observed in our measurements can be explained with a band model of the double junction structures by including the Schottky barrier for one junction and the vacuum gap as another. When the sample is biased positively in the n-type case, the metal–semiconductor interface is reverse biased as shown in Fig. 6(b). It should also be noted that most of the bias voltage is applied on the vacuum gap, i.e., $V_1 > V_2$ at all times.[23] The reverse biased Schottky barrier height does not change significantly as the voltage is swept. Therefore the established tunnel barrier height is almost constant throughout the voltage sweep in reverse bias. However when the polarity is reversed as in Fig. 6(c), the

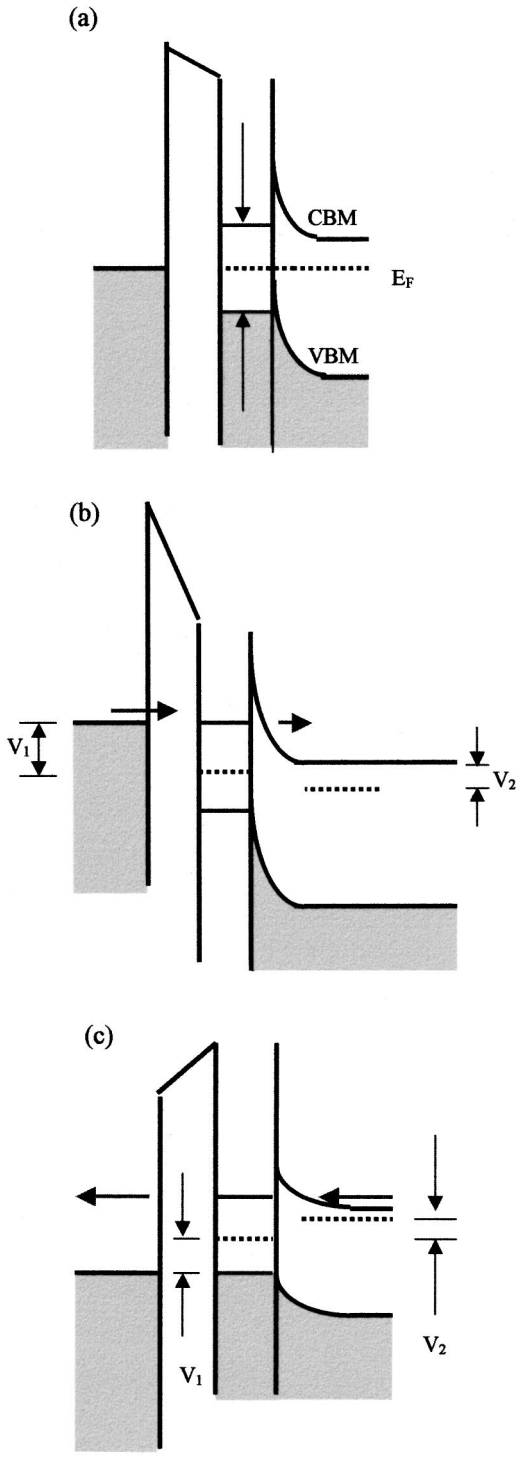

FIG. 6. Schematics of the tip–island *n*-type Si band structure (a) with no bias in equilibrium, (b) with positive sample bias (the metal-semiconductor interface is reverse biased), and (c) with negative sample bias (the metal–semiconductor interface is forward biased).

Schottky barrier is in forward bias, and thermionic emission is enabled in forward bias. For the *p*-type substrate, the situation is reversed. The Schottky barrier is forward biased when the sample is positively biased. This argument explains the trend displayed in Fig. 3, where conductance peaks are more obvious on the reverse biased side for *p*- or *n*-type substrates.

As we add an undoped silicon layer between the silicide island and the doped substrate, more conductance peaks appear on the reverse biased side while peaks on forward bias also become visible. We consider two possible explanations for this behavior in terms of the resistance and the capacitance, respectively. First, we are increasing the resistance of the metal–semiconductor tunnel barrier by adding an intrinsic silicon layer. Even though the total resistance of the system did not increase significantly compared with the case of no silicon layer, the resistance between the island and the substrate is expected to increase slightly. The increased electron confinement time in the island will therefore lead to the observation of more conductance peaks in both polarities.

Another argument is in terms of the capacitance of the island. The capacitance of the island can be estimated assuming the island as a sphere between a conducting plane (substrate) and another sphere (the STM tip). The approximate solution to the sphere–plane capacitance is

$$C(R,s)=2\pi\epsilon R(2+R/s),$$

where R is the radius of the sphere and s is the distance between the sphere and the plane.[24] As the distance between the island and the substrate increases, it results in a decrease of the island capacitance. In addition, the total capacitance of the island in our system includes depletion capacitance of the space charge region, which is dependent on the bias voltage. When the bias voltage is increased the total capacitance, which is given as a series combination of the geometric capacitance and the depletion capacitance, will decrease also. This reduces the capacitance of the island and makes the charging energy larger.

Even though the exact role of the intrinsic layer is not clear at this time, the above arguments and experimental observation tend to agree. Future experiments, which explore the thickness dependence of the intrinsic layer, could help determine which effect is dominant.

In a second study of $TiSi_2$ islands, our conducting tip atomic force microscopy results indicate that the Schottky barrier between the islands and Si substrate is not dependent on size, but shows substantial variation in barrier height (from 0.58 to 0.43 eV).[25] This variation has been related to the interface structure of the $TiSi_2$ islands. It is evident that this variation will limit device applications where reproducible characteristics are necessary.

Another aspect that has been ignored in our analysis is the effect of the surface potential around the edges of the islands. Analysis of the Schottky barrier variations for a metal–semiconductor interface indicates that nanoscale regions of low barrier height could be ''pinched off'' because of the surrounding high barrier regions. A similar effect could be present in the measurements presented here since the Si surface states will pin the surface Fermi level. Thus the space charge region under the islands could be affected. However, the measurable differences due to the different substrates suggests that these space charge effects could be relatively insignificant.[26]

B. Estimates from simple model and fitting

As noted above, we can model the tip–island–substrate structure as a pair of tunnel junctions in series. Each tunnel junction is modeled as a combination of a resistor and a capacitor in parallel. From the value of the distance of the steps in Figs. 4(a) and 4(b), $\Delta V \sim 0.5$ V, we can estimate the total capacitance for the tip–island–substrate system as $C_{\text{total}} = e/\Delta V \sim 3.2 \times 10^{-19}$ F. We also note that from the point of view of the charge on the island, two capacitors are connected in parallel. Assuming the island as a perfect sphere in vacuum with a diameter of 4 nm, we can estimate the lower limit of the total capacitance of the island to be $C_{\text{total}} \sim 2.2 \times 10^{-19}$ F, which is given by the self capacitance of a sphere in free space $C = 4\pi\epsilon_0 R$. Obviously, in our situation we will obtain a higher value. For the tip and island, C_1 can be estimated using the image charge method assuming two spheres with the same radius.[27] This gives a value of $C_1 \sim 5.8 \times 10^{-19}$ F for a 4 nm diameter and a 1 nm separation. On the other hand, assuming a sphere and a plane for the island–substrate junction, the C_2 is found as $\sim 4.4 \times 10^{-19}$ F for a sphere with a 4 nm diameter and a 1 nm separation.[24] Thus $C_{\text{total}} = C_1 + C_2$ from this calculation is found to be 1.0×10^{-18} F which is somewhat higher than the value of self-capacitance and the experimental value. This approach gives reasonable agreement despite the crude assumptions.

Another requirement for the charging effect is that both R_1 and R_2 are larger than the quantum of resistance 25.8 kΩ and their magnitudes should be asymmetric to be able to observe the charging effect. We can estimate the R_{total} by inspecting the current at 2.5 V for example. The current value of 5 nA at this voltage gives $R_{\text{total}} \sim 500$ MΩ. Our conducting AFM measurements in contact on a larger island ($d \sim 0.1$ μm) gave a contact resistance R_2 on the order of several MΩ. Since $R_{\text{total}} = R_1 + R_2$, we can approximate that $R_{\text{total}} \sim R_1$. This satisfies not only the requirement for a long lifetime of the trapped electron, but also the asymmetry of the junctions ($R_1 C_1 \gg R_2 C_2$) that is necessary for the observation of the Coulomb staircase.

V. CONCLUSIONS

We have successfully fabricated nanoscale $TiSi_2$ islands on an atomically clean Si(111) 7×7 surface. The island size distributions are dependent on processing parameters such as the initial deposition thickness, and the annealing temperature and time. Islands of ~5 nm diameter showed Coulomb blockade and Coulomb staircase effects at room temperature. These phenomena can be explained in terms of single electron charging of a metallic island in the tip–island–substrate double junction system.

ACKNOWLEDGMENT

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