MORPHOLOGY OF SILICON OXIDES ON SILICON CARBIDE

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ABSTRACT

The development of high power devices based on silicon carbide requires a more complete understanding of the oxide formation process and interface characteristics. By using an integrated UHV system, samples were cleaned and oxides deposited *in situ*. The approach of the oxide formation process was to form the initial insulator, a few angstroms thick, and then deposit an oxide. Various deposition techniques are used in the oxide growth process; both thermal and plasma enhanced chemical vapor deposition were employed with two different precursors (oxygen and nitrous oxide), and the results were compared with thermal oxidation. The morphology of each of the deposited oxides was compared to the bare substrate and the thermal oxide wafers. This study focuses on the morphology of the different deposition processes using AFM. Examination of the morphology of the initial insulator growth process and the oxide deposition process gives insight into the physical characteristics of the silicon dioxide deposited on silicon carbide. The RMS values of the initial insulator formation and the control wafers are 0.93 and 0.95 nm respectively. Meanwhile, the RMS values for PECVD (200-400°C) and thermal CVD (400-600°C for oxygen-silane and 800-1000°C for nitrous oxide-silane) range from 1.43 to 1.93 nm.

INTRODUCTION

Wide bandgap semiconductors are increasingly being considered in semiconductor applications that require high temperatures and high breakdown characteristics. With the improvement and availability of SiC wafers, the material is now considered to be most promising material for high power semiconductor applications. Another advantage of SiC over other compound semiconductors is that it has a native oxide. However, significant problems persist with the thermal oxidation of p-type SiC. The dopant in p-type SiC (B or Al) is incorporated into the grown oxide, generating traps and fixed oxide charge [1,2]. Because of this phenomenon, there is a need to develop new processes for preparing gate dielectrics. Our approach is to circumvent the problem of dopant redistribution by using deposited oxides as a gate dielectric. The morphology of these deposited oxides becomes a matter for concern. In this study, the morphology of the deposited oxides is compared to that of thermally grown oxides to determine if the deposited oxides are a viable alternative to thermal oxidation for gate dielectric applications.

EXPERIMENT

The substrates used were partial wafers of p-type 4H-SiC 8 off axis with a 4.5 m epitaxial layer supplied by Cree Research Inc. The samples were wet chemically cleaned using a SC1 etch (5:1:1 H_2O:NH_4OH:H_2O_2) at 80C for 10 min followed by 5 min DI water rinse, and then a SC2 etch (5:1:1 H_2O:HCl:H_2O_2) at 80C for 10 min followed by 5 min DI water rinse [3,4]. The final wet chemical step was a series of UV/Ozone exposures followed by 10:1 HF dips. Samples were then divided into two batches. The first batch would be processed in quartz tube furnaces, while the second was processed in a UHV oxide deposition system. Samples processed in the UHV oxide deposition system had tungsten sputtered on the backside using an argon sputterer. The

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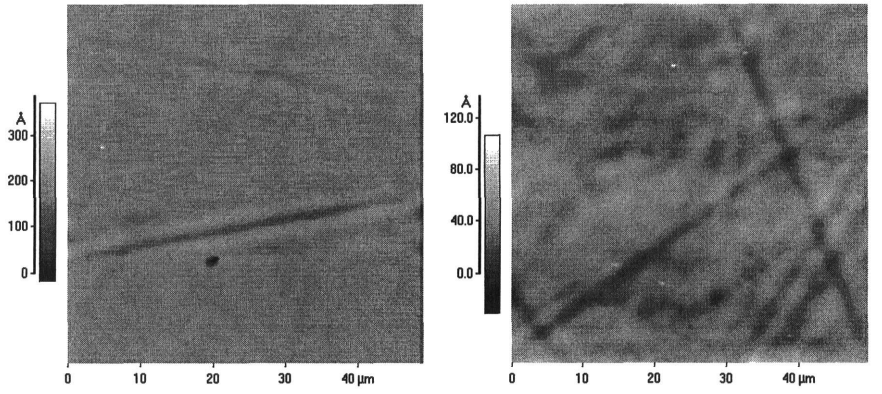
tungsten deposited on the backside acts as an absorber for radiative heating. All samples were then cleaned using a UV/Ozone exposure followed by a 10:1 HF dip. Atomic force microscopy (AFM) was then performed on a series of samples to obtain an overall view of the surface roughness before oxide deposition. After the AFM measurements, all samples were cleaned with a UV/ozone exposure to remove any surface contaminants due to ambient exposure. The samples were then dipped in 10:1 HF and exposed to a buffered oxide etch (BOE) vapor. By holding the sample a few millimeters above a solution of BOE for several minutes the BOE vapor treatment decreases the surface carbon contamination, and increases the fluorine adsorbtion on the surface. This is a desired quality since the fluorine populates some sites that residual oxygen would populate and it is readily desorbed at low temperatures.

Samples with tungsten on the backside were loaded into a UHV transfer mechanism (base pressure of 1 x 10^{-9} Torr) which has a series of stations for cleaning, analysis, and oxide deposition. The samples were then cleaned in a hydrogen plasma system (base pressure of 1 x 10^{-9} Torr) which has been shown to remove surface organics and hydrocarbons [5]. Auger analysis before and after hydrogen plasma cleaning shows residual oxygen on the surface. The residual oxygen was not removed for this study. Likewise, the loaded samples exhibited no LEED pattern for moderate beam energies (<250 eV) while the hydrogen plasma cleaned samples exhibit a sharp 1 x 1 LEED pattern at low beam energies (<50 eV). The samples were then transferred into the oxide deposition system (base pressure 1 x 10^{-8}). A tungsten coil radiative heater below the sample was used to heat the substrate. In the oxide deposition system, a variety of processes may be used to deposit oxides. PECVD oxides were deposited by exciting O_2 or N_2O in a quartz tube located 10 cm above the sample with a 13.56MHz RF generator. 1% SiH_4 in hydrogen is introduced just above the sample and not excited in the plasma [6]. Oxide thicknesses of approximately 400Å were deposited in 5 min. LPCVD oxides were also deposited in the oxide deposition system. These were deposited using O_2 and 1% SiH_4 in hydrogen at 550° for 60 min or N_2O and 1% SiH_4 in hydrogen at 750° for 40 min [7]. The samples were then removed and some were selected for annealing in a rapid thermal annealer (RTA) at 1000°C for 60 sec to densify the deposited oxides. Others were used to obtain the morphology of the PECVD and LPCVD oxides.

Samples that were processed in the quartz tube furnaces did not have tungsten deposited on the backside to avoid contamination of the furnaces. The substrates were again divided into two subsets. A 450Å thick low temperature oxide (LTO) was deposited on the first subset of substrates. The oxide was deposited at 400C using diethylsilane (LTO-410) and oxygen precursors. This deposition system is a horizontal, low pressure CVD system in which the SiC substrate lies flat. After the oxide deposition a set of samples was selected for annealing using a RTA at 1000°C for 60 sec. The second subset of substrates was thermally oxidized at 1 ATM. in pyrogenic steam at 1050°C for 120 min. Following the deposition, the wafers were subjected to a post oxidation anneal at 900°C in N_2 for 60 min [8]. The thermal oxidation was completed in a horizontal Tytan II three-zone furnace in which the SiC substrate lies flat. The oxidized wafers were then examined by AFM to determine the surface morphology.

RESULTS

The morphology of the SiC was examined prior to oxide deposition. The range of root mean square (RMS) roughness values from AFM on cleaned substrates is 0.95nm to 1.36nm. These values serve as the benchmark for determining whether or not the surface morphology of the deposited oxide is an issue for the quality of the oxides. The surface roughness of samples with and without tungsten sputtered on the backside (figure 1a & 1b) are nearly identical.



1a 1b

Figure 1. AFM of cleaned substrate (a) without tungsten on the backside, (b) with tungsten on the backside

The substrates with tungsten on the backside exhibit a RMS roughness of 1.13 nm; while the substrates without tungsten deposited on the backside showed a roughness of 1.87 nm. Since the RMS roughness between the two is less then 1 nm, it is resolved that the tungsten backside contact has little to no affect on the surface morphology of the sample.

The polishing scratches are very prevalent. The scratches are about 10 nm peak to valley on the cleaned wafers. The thermal oxide wafers show little change from the cleaned wafers. The roughness of the thermal oxide samples is 0.93 nm (figure 2), and the peak to valley height of the scratches is still about 10 nm.

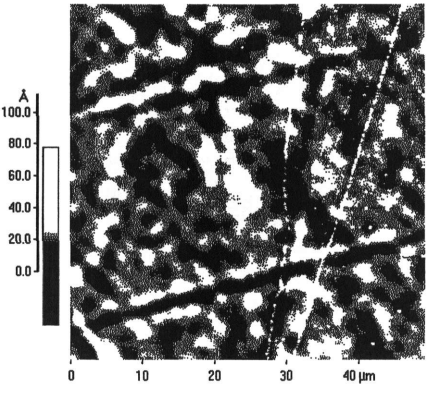
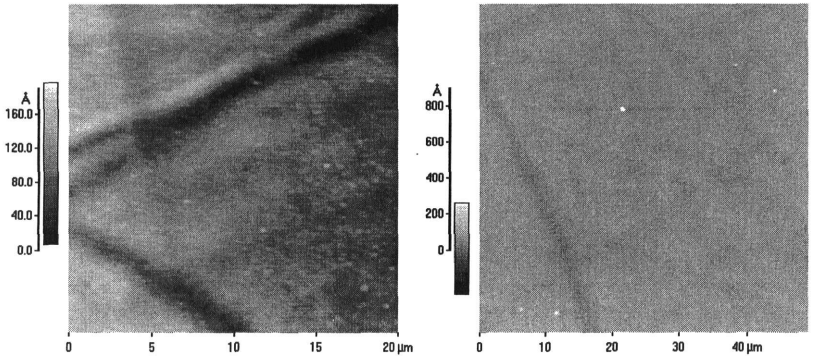


Figure 2. AFM of Thermal Oxide grown at 1050C for 2 hr.

These polishing scratches are not removed by the sacrificial thermal oxidation and may be a concern for gate dielectric quality. Furthermore, after an initial plasma oxidation, via O_2 or N_2O plasma, the morphology of the bare substrate and the initial plasma insulator are identical. The polishing scratches are too pronounced to be removed by a short plasma treatment or thermal oxidation.

Since PECVD oxides require the lowest thermal cycle, it may be a preferred process for gate oxide deposition. After a PECVD oxide deposition, the RMS surface roughness increases to between 2.1 to 2.3 nm. The roughness is reduced to 1.43 to 1.74 nm after a RTA (figure 3a & 3b).

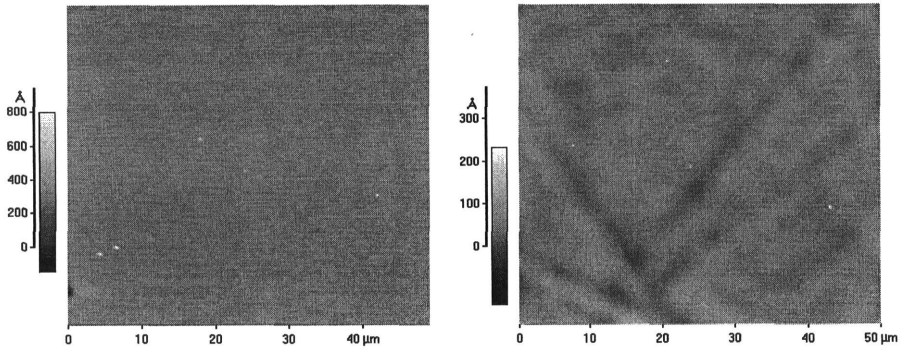


3a 3b

Figure 3. AFM of PECVD oxides (a) before RTA, (b) after RTA

A reduction of approximately 5Å RMS roughness is observed after a 60 sec densification of the oxide at 1000C. The densified PECVD oxide roughness is essentially equivalent to the substrate roughness. The polishing scratches are also prevalent through the PECVD deposited films. The scratches are of the same depth as the cleaned substrates. Therefore, the PECVD densified oxide does not significantly change the surface morphology of the substrate, and does not lessen the depth of the polishing scratches.

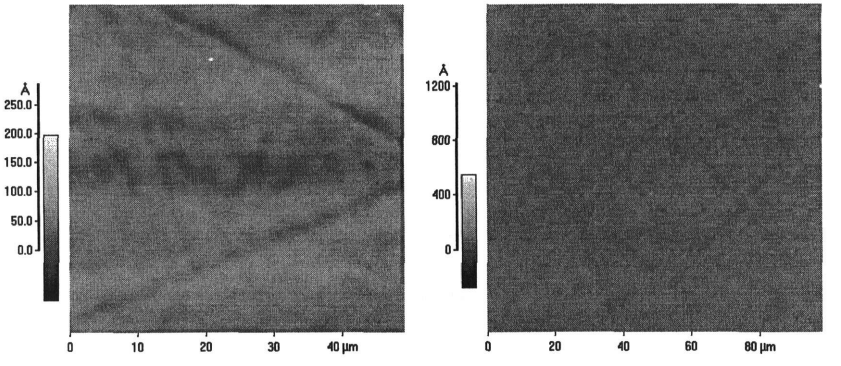
Likewise, the LPCVD oxides (figure 4a & 4b) have RMS roughness of 2.55nm, which is slightly reduced to 1.99nm after RTA. Again, the densified oxide RMS roughness is essentially equivalent to the substrate roughness. The LPCVD films exhibit the same overall RMS roughness as the SiC wafer, and the polishing scratches are still prevalent, and undiminished.



4a 4b

Figure 4. AFM of LPCVD Oxides (a) Before RTA, (b) after RTA

LTO deposited oxides exhibit similar behavior (figures 5a & 5b). The LTO deposition process does not appear to roughen the surface morphology. The before and after RTA RMS roughness (1.38 nm and 1.02 nm respectively) correspond to the RMS values for the cleaned substrates. The LTO process is typically used as a final passivation layer. It is shown that the LTO process does not affect the depth and roughness of the polishing damage.



5a 5b

Figure 5. AFM of LTO (a) before RTA, (b) after RTA

The LTO, PECVD, and LPCVD deposited oxides do not significantly increase the RMS roughness of the wafer surface. The polishing scratches are evident even after the oxide deposition or the thermal oxidation. The polishing scratches are still the most noticeable cause

for surface roughness. The scratches are about 1/4 of the thickness of the gate dielectric. While the scratches are evident, the films deposited by PECVD, LPCVD, and LTO demonstrate that smooth surfaces may be obtained from a smooth starting surface. Therefore, deposited oxide morphology is expected to have little effect on the quality of the gate dielectric.

CONCLUSIONS

Deposited oxides on silicon carbide can be prepared without significantly increasing the surface roughness. The roughness is not significantly reduced by thermally oxidizing the wafer. For PECVD films, it was found that a 1 min rapid thermal anneal at 1000°C is sufficient to lower the RMS roughness to within 1nm of the substrate roughness. With no significant roughening of the surface by PECVD or LPCVD of oxides on silicon carbide, deposited oxides may be a viable alternative to thermal oxidation for gate dielectrics. The morphology of deposited oxides is expected to have little to no effect on electrical characteristics of devices on silicon carbide. However, the polishing techniques for silicon carbide need to be improved. The polishing scratches propagate through the epi-layer and the deposited and thermal oxides. The depth of these scratches is of the order of the gate thickness. The depth of the scratches must be reduced to assure a smooth surface for processing.

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