Influence of Dry and Wet Cleaning on the Properties of Rapid Thermal Grown and Deposited Gate Dielectrics

XIAOLI XU, RICHARD T. KUEHN, MEHMET C. ÖZTÜRK, and JIMMIE J. WORTMAN

Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695-7911

ROBERT J. NEMANICH

Department of Physics, North Carolina State University, Raleigh, NC 27695-8202

GARI S. HARRIS and DENNIS M. MAHER

Department of Material Science and Engineering, North Carolina State University, Raleigh, NC 27695-7916

Various silicon surface cleaning processes for rapid thermal in-situ polysilicon/oxide/silicon stacked gate structures have been evaluated. Metal-oxide-semiconductor capacitors were fabricated to assess the effects of cleaning on the quality of gate oxide structures produced by both rapid thermal oxidation (RTO) and rapid thermal chemical vapor deposition (RTCVD). Excellent electrical properties have been achieved for both RTO and RTCVD gate oxides formed on silicon wafers using either an ultraviole/zone (UV/O_3) treatment or a modified RCA clean. On the contrary, poor electrical properties have been observed for RTO and RTCVD gate oxides formed on silicon wafers using a high temperature bake in Ar, H_2, or high vacuum ambient. It has also been found that the electrical properties of the RTCVD gate oxides exhibit less dependence upon cleaning conditions than those of RTO gate oxides. This work demonstrates that initial surface condition prior to gate oxide formation plays an important role in determining the quality of RTO and RTCVD gate oxides.

Key words: Metal-oxide-semiconductor, rapid thermal chemical vapor deposition, rapid thermal oxidation, surface clean

INTRODUCTION

Low thermal budget, ultraclean environment, and controlled surface chemistry are required in order to realize ultra-thin gate dielectrics with low defect density and high dielectric breakdown strength for advanced device applications. High vacuum in-situ rapid thermal processing (RTP) systems show promise for producing ultra-thin oxides with reduced thermal budget and reduced process-induced microcontamination.[1,2] In an RTP system, stacked polysilicon/oxide/silicon gates can be formed in-situ within a few minutes without exposure to atmosphere. In addition, since RTP systems are cold-walled, depositions on the chamber wall and particulate generation in the reaction chamber are minimized. Silicon wafer cleaning has received considerable attention for silicon epitaxy.[3,4] However, the influence of different silicon wafer cleaning methods on the properties of the gate dielectrics still remains an important issue to be addressed. In this work, we utilize an RTP system to investigate the effects of various (dry and wet) surface cleaning procedures on the quality of both rapid thermal oxidation (RTO) and rapid thermal chemical vapor deposition (RTCVD) oxides using in-situ polysilicon/oxide/silicon metal-oxide semiconductor (MOS) capacitors. The basic approach is to examine the properties of RTO and RTCVD gate oxides with different initial surface conditions created by different cleaning procedures. These surface conditions (prior to gate oxide formation) include: 1) a silicon surface with an initial oxide film generated using either wet chemical modified RCA clean or exposure to UV/O_3; 2) a silicon surface with initial oxide removed using in situ high temperature bake in Ar, H_2, or high vacuum; and 3) a silicon surface with hydrogen termination formed by a hydrofluoric acid (HF) treatment.

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EXPERIMENTAL

As mentioned, the two oxide processes considered are RTO and RTCVD. The RTP system used is a cylindrical quartz reaction chamber with cold walls, a load lock, and oil-free pumps (with base pressure of 10^{-8} Torr).[5] Temperature ramp up was carried out in oxygen for RTO and in a mixture of SiH_4/Ar and N_2O for RTCVD oxide. The reactant gases were directed axially down the tube over a wafer aligned parallel to the gas flow. The wafer was loaded with the polished surface facing down in order to reduce particle contamination.[6] The wafer was supported on the edge by short quartz legs that are mounted on a quartz holder. Boron-doped (0.5 Ω-cm), 4-inch silicon wafers with (100) orientation were used as the substrate material. A field oxide of approximately 3000Å was grown in steam at 950°C, and the active area was then defined by photolithography and wet etching. Prior to gate oxide formation, wafers were treated using different dry and wet surface cleaning procedures as summarized in Table I. Gate oxide films with thicknesses ranging from 70 to 105Å were formed using RTO and RTCVD separately. The RTO was grown at a temperature of 1050°C and at a pressure of 760 Torr. The RTCVD oxide was deposited by reacting SiH_4 (10% diluted in argon) and N_2O at a temperature of 800°C and at a pressure of 3 Torr with a SiH_4/N_2O flow rate ratio of 4%. After the gate oxide formation, the system was pumped down to 10^{-7} Torr to minimize the effects of residual gases on the following in-situ polysilicon deposition. Polysilicon film (2000Å) was then deposited on the gate oxide.[5] Secondary ion mass spectroscopy (SIMS) analysis result shows that the relative oxygen concentration in the polysilicon film is less than 0.2%. Polysilicon film was subsequently ex-situ doped using $POCl_3$ at 900°C. Aluminum was then evaporated and all samples were annealed in forming gas at 400°C for 30 min. Capacitors with areas ranging from 4×10^{-4} to 2.5×10^{-3} cm^2 were used for the study. The gate oxide thicknesses were measured using a capacitance-voltage method.

Table I. Final Surface Cleaning Prior to RTO and RTCVD Oxide Formation

I	Modified RCA* + 1050°C bake in Ar
II	Modified RCA + 1050°C bake in H_2
III	Modified RCA + 1050° bake in high vacuum (10^{-8} Torr)
IV	Modified RCA + UV/O_3 (5 min)
V	Modified RCA + 1% HF spin
VI	10% HF dip + Modified RCA

*Modified RCA: H_2O_2 + NH_4OH (5 min), H_2O_2 + HCl (5 min), T = 70°C.

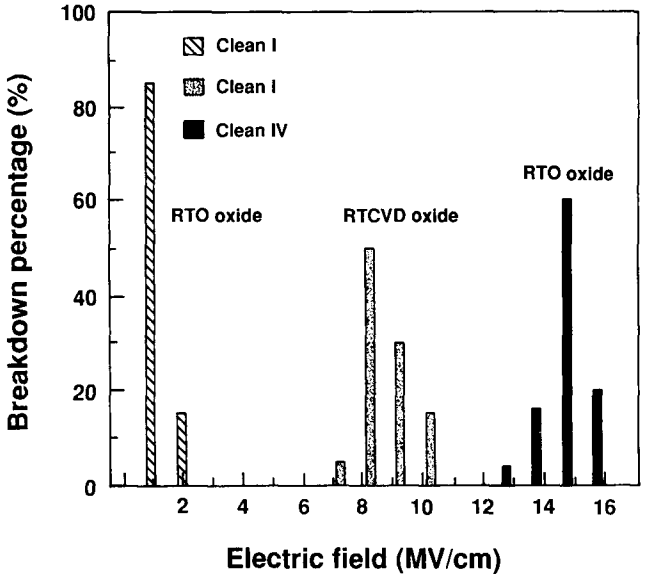

Fig. 1. Comparison of breakdown histograms of RTO and RTCVD gates with different dry cleaning procedures.

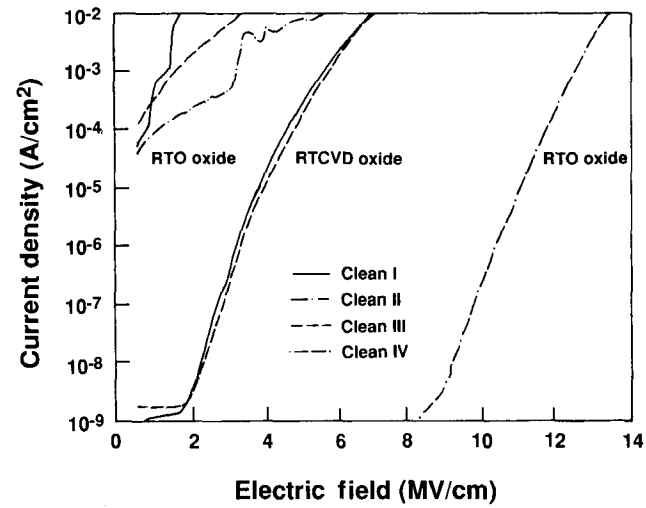

Fig. 2. Current density as a function of electric field for RTO and RTCVD gates with different dry cleaning procedures.

RESULTS AND DISCUSSION

Breakdown field measurements were made for both RTO and RTCVD gate oxides with different final dry and wet surface cleaning treatments. The breakdown voltage of the gate oxide is determined from the current (I)-voltage (V) characteristics using a voltage ramp method. In this method, the applied voltage is increased in an accumulation mode for the p-type substrate at a ramp rate of approximately 0.5 V/sec until a sufficient current density of 2.5 A/cm^2 is reached. The corresponding voltage (V_B) is recorded. After the above test, the current density of the sample is measured again at half the recorded voltage (0.5 V_B). If this re-measured current density is higher than the specified value (2.5 A/cm^2) (which indicates nonreversible I-V characteristics of the gate oxide), the previously recorded voltage (V_B) is defined as the catastrophic breakdown voltage. In this study, the catastrophic breakdown voltage divided by the oxide thickness is defined as the oxide breakdown field. Fifty capacitors were tested across the wafer for each clean condition. Figure 1 compares the catastrophic breakdown histograms of MOS capacitors with final dry cleaning procedures I and IV for both RTO and

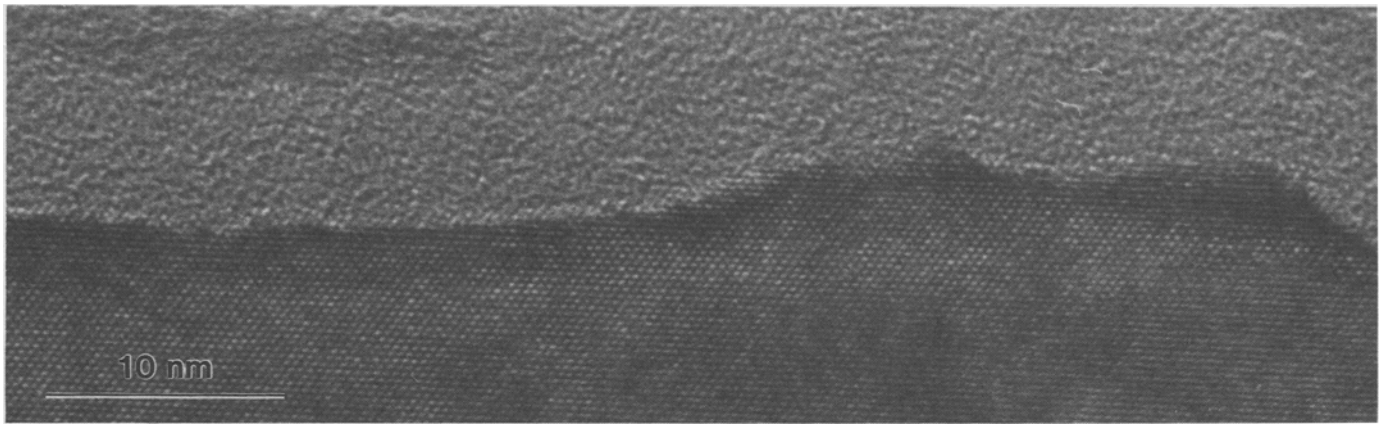

Fig. 3. High resolution TEM image of RTO oxide formed after modified RCA clean followed by 1050°C high vacuum (10^{-8} Torr) bake.

RTCVD gate oxides. As shown, the modified RCA clean followed by a 1050°C argon bake (clean I) results in a very low breakdown field (~1MV/cm) for the RTO oxides. Similarly, a modified RCA clean followed by a high temperature (900°C) bake in H_2 (clean II) or high vacuum (1050 °C, clean III) (not shown) also leads to a poor breakdown characteristic for the RTO oxides. Figure 2 shows the current density as a function of electric field for samples treated using final dry cleaning methods I–IV, which consistently supports the above observations. High temperature process-induced-defect microchemistry in SiO_2/Si structures has been studied previously.[7–10] It has been found that under a low O_2 concentration condition, there exists an interfacial decomposition for the silicon wafer with a SiO_2 layer:

$$Si + SiO_2 \rightarrow 2SiO \quad (1)$$

The SiO is volatile at temperatures above 750°C. As soon as the SiO_2 film is removed, an etching of silicon for the silicon wafer without a SiO_2 layer is established:

$$2Si + O_2 \rightarrow 2SiO \quad (2)$$

This is because there is a boundary of O_2 partial pressure between the growth of SiO_2 and etching of the silicon via the formation of a volatile SiO. The critical partial pressure of O_2 at a temperature of 900°C is approximately 1×10^{-2} Torr for silicon wafers with (100) orientation.[8] If the partial pressure of O_2 is below this value, high temperature (≥ 900°C) dry cleaning will etch silicon surface instead of growing oxide. It is very likely that the modified RCA clean followed by a high temperature bake (≥ 900°C) in Ar or H_2 (with impurity O_2 < 1 ppm), or high vacuum ambient (10^{-8} Torr) will first initiate the interfacial decomposition reaction (1) at Si/SiO_2 interface and remove the SiO_2 layer produced by the modified RCA clean. This reaction is then followed by silicon surface etching process of reaction (2). As an example, Fig. 3 shows notable interface roughness as high as 50Å for samples treated using modified RCA clean followed by 1050°C high vacuum bake (10^{-8} Torr). Therefore, a high temperature bake (≥ 900°C) in Ar or H_2 (with impurity O_2 <1 ppm) or high vacuum ambient (with pressure of 10^{-8} Torr) can generate a high density of microdefects and roughness on the silicon surface, which can result in a high leakage current in the subsequently formed RTO gate oxides.

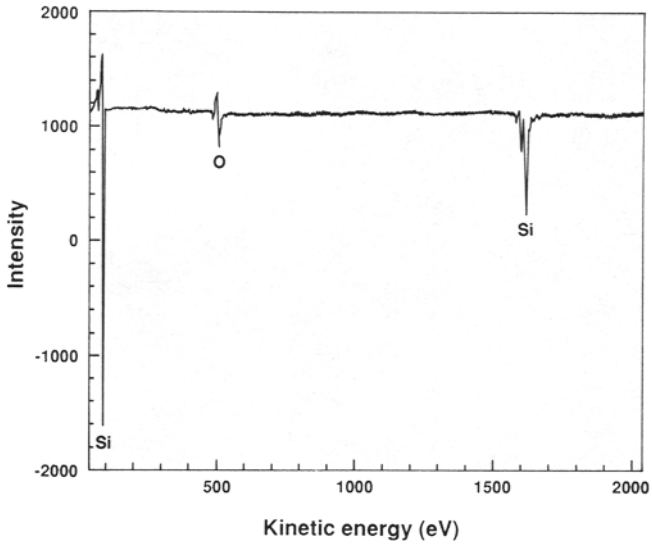

Fig. 4. Auger electron spectroscopy of silicon surface after final UV/O_3 treatment.

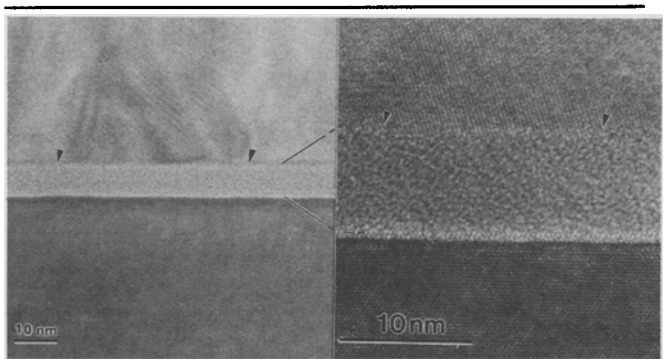

Fig. 5. High and low magnification TEM images of polysilicon/RTO oxide/silicon stacks formed after final UV/O_3 treatment.

On the other hand, when we employ a modified RCA clean followed by an ex-situ UV/O_3 treatment (clean IV) before RTO or RTCVD gate oxide formation, excellent breakdown characteristics were ob-

tained. Figures 1 and 2 show that high breakdown field with very low leakage current density is obtained for RTO gates using a modified RCA clean followed by an UV/O_3 treatment. We did not observe oxide breakdown for an electric field up to 12 MV/cm. Figure 4 shows an Auger electron spectroscopy (AES) of the silicon surface after a modified RCA clean followed by an ex-situ UV/O_3 treatment. No surface contamination (such as carbon) is detected within the sensitivity of AES analysis (1%). Figure 5 shows high and low magnification transmission electron microscopy (TEM) images of the polysilicon/RTO oxide/silicon stacks. This RTO oxide is grown following a final UV/O_3 treatment. As shown, atomically flat interface between the RTO oxide and the silicon substrate is obtained. These observations indicate that weak spots resulting from surface contamination or microroughness from surface etching are not responsible for the breakdown behavior of the UV/O_3 treated RTO gates. This is attributed to the fact that most of the surface contaminants such as hydrocarbons are removed through the excitation or dissociation of species by absorption of the ultraviolet light. The modified RCA clean and UV/O_3 treatment produce an initial oxide on the silicon surface (Fig. 4), thus effectively suppressing microdefects in the subsequently formed RTO gate oxide.

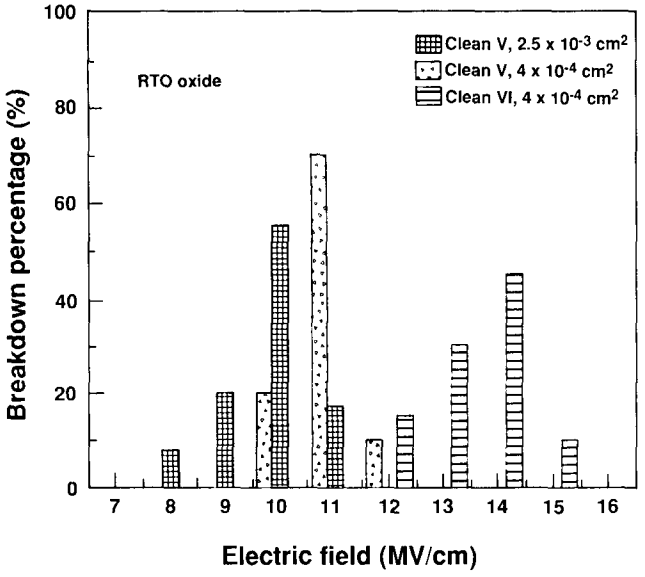

Fig. 6. Comparison of breakdown histograms of RTO gates with different wet cleaning procedures (cleaning methods V and VI) and different capacitor areas (cleaning method V).

It is interesting to note that in Figs. 1 and 2, RTCVD gate oxides deposited after a high temperature bake in argon have a higher average breakdown field and a lower leakage current density than those of RTO grown after the same surface treatment. Similar results have been observed for RTCVD oxide using a high temperature (1050°C) bake in high vacuum (Fig. 2). This can be attributed to the fact that RTCVD oxide is formed by deposition rather than diffusion. The microcontamination (absorbed through the chemical solution and ambient air) or microdefects produced by high temperature etching under low O_2 partial pressure will be covered by the RTCVD oxide films. Therefore, the electrical quality of such deposited oxide is less dependent on the microdefects or roughness generated during previous high temperature bake processes. Our experimental results also show that even though the quality of the RTCVD oxide is much better than that of RTO formed under the same high temperature pre-bake condition, it is not as good as that of RTCVD oxide formed after employing final UV/O_3 treatment or a final modified RCA clean.

The results of catastrophic breakdown field measurements for RTO and RTCVD gate oxides using final wet chemical cleaning methods including HF

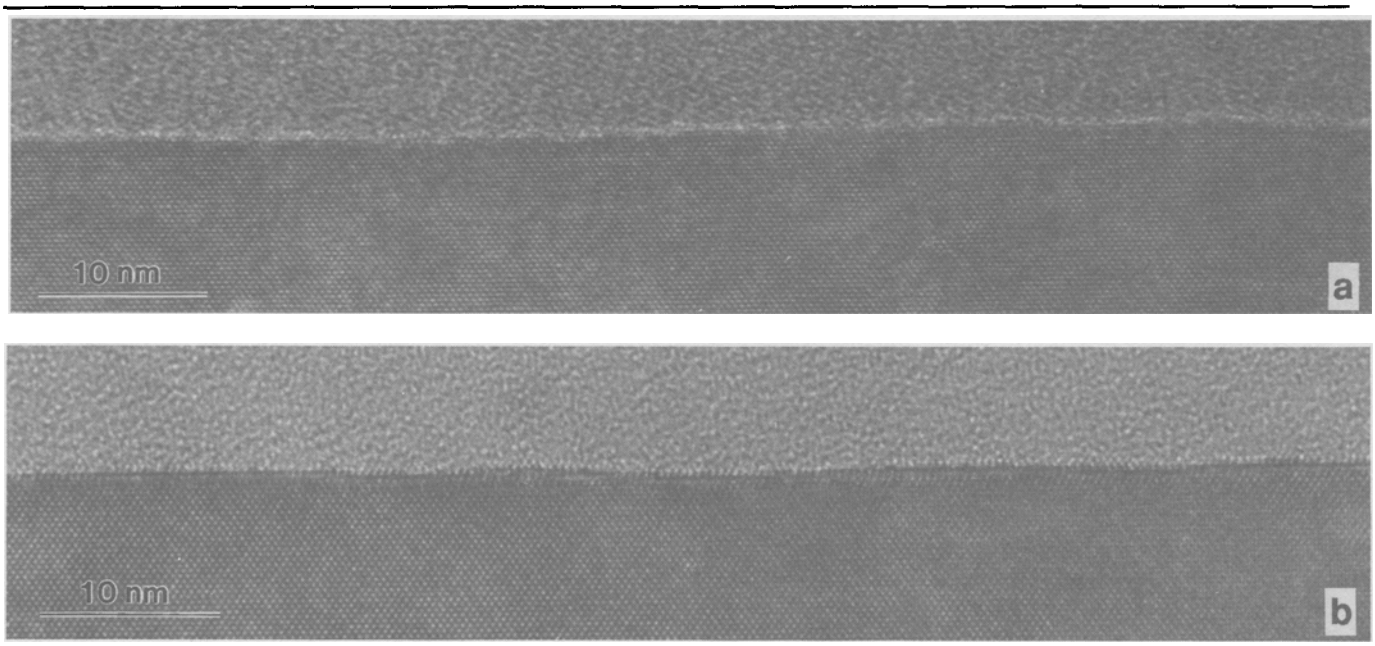

Fig. 7. High resolution TEM images of RTO oxide formed after final HF spin (a) and final modified RCA clean (b).

spin (clean V) and modified RCA (clean VI) are shown in Fig. 6. The catastrophic breakdown field dependence on capacitor area can be seen by comparing the different areas for the cleaning method V (modified RCA + 1% HF spin). Similar pattern for breakdown field dependence on capacitor area is observed for samples using final wet modified RCA treatment. It can be seen that, (1) as capacitor area increases, the average catastrophic breakdown field decreases, and (2) a slightly higher average breakdown voltage was obtained for the samples in which a final modified RCA treatment was used. A slight improvement in the leakage current was also found for these samples compared with those cleaned using a final HF spin. A possible explanation for this improvement for wafers using final modified RCA cleaning is that the modified RCA clean may effectively remove organic surface materials and metals through dissolution and result in an initial oxide passivated silicon surface.[11] The initial oxide passivated silicon surface is less susceptible to further contamination and will be more stable during subsequent rapid thermal processing. However, an HF treatment after the modified RCA clean will remove the passivated oxide film on the surface and generate a hydrogen terminated surface. It is known that this hydrogen termination on the silicon surface decomposes at a temperature of approximately 450°C, resulting in dangling-bond sites on the surface.[12] During the rapid thermal processing to form gate oxides (temperature ≥ 800°C), contaminants resulting either from chemical solutions used during wet cleaning procedures, from ambient air during wafer transport and handling, or from residual impurities in the processing chamber are more likely to be attached to the exposed dangling-bond sites, thus, leading to a decreased breakdown voltage in the subsequently formed gate oxides. The possibility also exists that HF treatments cause microroughening of the oxide/silicon interface that could lead to degraded breakdown voltage. However, our TEM analysis results show that there is no substantial difference in the oxide/silicon interface roughness between wafers treated using a final HF clean (Fig. 7a) and wafers treated using a final modified RCA clean (Fig. 7b).

SUMMARY

The presented results indicate that gate oxides produced by either RTO or RTCVD on silicon surfaces with an initial oxide result in low defect SiO_2/Si structures. In contrast, if the initial oxide is removed in-situ by a high temperature bake or HF treatment, the resulting SiO_2/Si structure shows an increased leakage current and reduced breakdown voltage. These degradation properties are due to either surface roughening or surface defects resulting from etching or contaminant incorporation. It is also shown that RTCVD oxides formed on silicon surfaces with initial oxide removed lead to better electrical characteristics than those of RTO oxides after the same dry cleaning treatment at high temperature. It is worth drawing a comparison to silicon epitaxy processes. It is known that good quality of epitaxial silicon layer can be obtained only after removal of the initial oxide passivation film. This is accomplished either by high temperature bake in Ar, H_2, or high vacuum[3,4] or by an HF treatment.[13] Our experimental results show that for RTO and RTCVD gate oxide formation, the surface conditions such as roughness and contamination are critical in SiO_2/Si interfaces, and cleaning techniques conventionally used for silicon epitaxial processes are not necessarily applicable to rapid thermal gate dielectric formation.

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