Materials and Processes for High k Gate Stacks: Results from the FEP Transition Center

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Materials and Processes for High k Gate Stacks: Results from the FEP Transition Center

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A wide variety of materials and processes for high k dielectrics and metal gate electrodes have been studied as replacements for poly-Si/SiO_2 or SiON in advanced CMOS devices. Care must be taken with the interfacial layer to control not only the nitrogen content but its spatial location. Nanocrystallization of the high k dielectric and the corresponding formation of charge and trapping levels associated with defects in the dielectric present one of the current challenges. Control of the workfunction of the gate electrode is shown to depend on many variables, including oxygen content and the material used for the capping layer on the metal gate. The hafnium oxide family of materials, along with metal alloy gates, is seen to provide the best solution for equivalent oxide thicknesses (EOT's) < 0.7 nm, but higher k dielectrics and thinner interfacial layers are needed below 0.7 nm.

Introduction

Considerable progress has been made over the last 5 years in identifying materials for high k gate stacks (1). Such systems require: i) interfacial layers to minimize interfacial charge in order to maximize channel mobility, ii) high k dielectrics whose barrier heights are sufficient to reduce tunneling leakage and which are resistant to charge trapping, and iii) metal gate electrodes having controllable workfunctions, e.g., dual band-edge for high performance bulk CMOS. Schemes for achieving low equivalent oxide thickness (EOT) are schematically illustrated in Fig. 1, where an additional interfacial layer between the high k dielectric and the metal gate may also be needed. The materials for these gate

stacks must be thermally and electrically stable, first with respect to the high temperatures encountered in normal integration schemes and, second, with respect to the high levels of charge injection and transport that occurs over a device lifetime. The Hf-Si-O-N dielectric on top of an interfacial oxide layer (2ML ~ 0.3nm EOT) continues to show great promise for applications in the 0.7-1.0 nm EOT range when used with metal gates. The choice of a suitable gate electrode material continues to be a challenge, in part because more emphasis has been placed on the dielectric and in part because electrode requirements differ from one application to another, and potential solutions range from poly-Si in low standby power applications, to (near) midgap materials (TiN, FUSI) for FDSOI and multi-gate, to bend edge metals for bulk high performance devices. Scaling EOT to 0.5 nm or below requires further reduction of the EOT of the interfacial layer and higher-dielectric-constant materials having lower leakage. This paper describes some of the learning about these materials obtained by the SRC/ SEMATECH Front End Process Transition Center (FEP TC) as we look forward to their introduction into mainstream technology in the not too distant future.

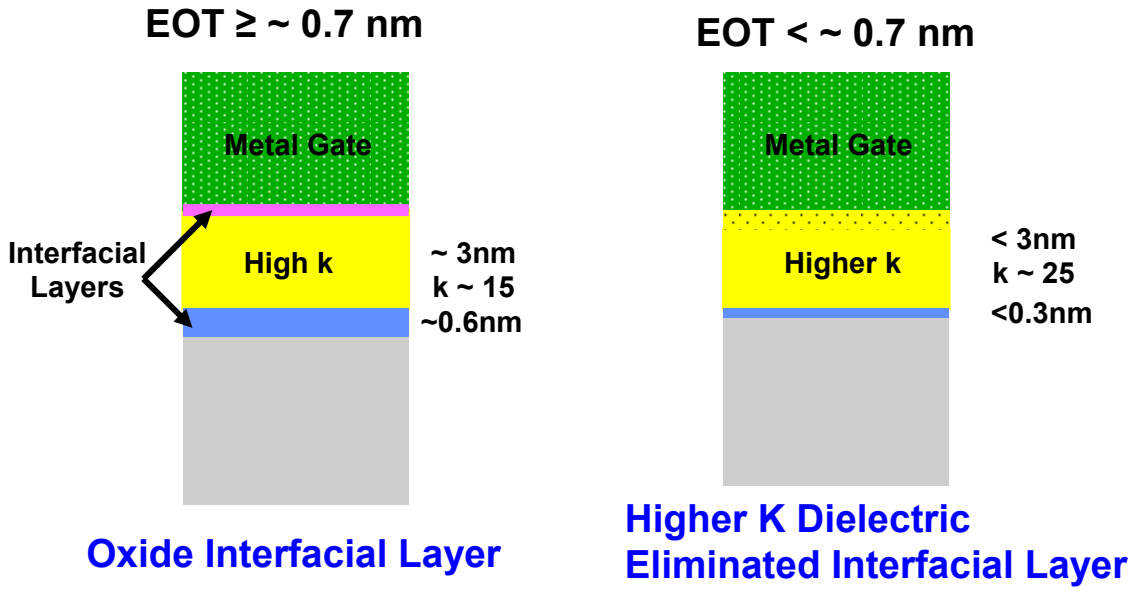


Figure 1. Schemes for achieving EOT ≥ ~0.7 nm (left) and EOT < ~0.7 nm (right)

Interfacial Layer

Interfacial Oxide Transition Layer

Control of the interfacial layer in contact with Si is the starting point for integration of high k gate stacks. The Si-SiO_2 interface in thermally-grown Si-SiO_2 gate stacks is the standard by which all gate stacks employing alternative dielectrics are measured. Several studies have established that the SiO_2 interface with Si produced by thermal oxidation is neither abrupt on atomic scale, nor strain free (2-4). Several theoretical studies have also found interfacial transition regions or ITRs to be an intrinsic bonding property of the Si-SiO_2 interface (5,6). Experimental studies based on medium energy ion scattering (MEIS) (2), spectroscopic ellipsometry (SE) (3), and synchrotron or soft x-ray photoelectron spectroscopy (SXPS) (4) have identified a thin ITR, ~0.3 to 0.4 nm thick with suboxide bonding arrangements. This thickness of this layer has been confirmed by high resolution transmission electron microscopy (HRTEM) studies (7), and SXPS (8). The ion

scattering studies have shown that the disordered region in the Si substrate, Si_D, is between 0.5 and 1.0 nm thick, or ~ 3 atomic layers. The thin ITR with suboxide bonding provides a strain reducing buffer layer between the crystalline Si (c-Si) substrate, and the more *elastically compliant* non-crystalline SiO_2 dielectric film. Several factors contribute to interfacial bond-strain and subsequent formation of the ITR. Differences in the Si-Si inter-atomic distances in the c-Si substrate, 0.235 nm, and the SiO_2 dielectric, ~0.305 nm, generate intrinsic compressive stress in the oxide and tensile stress in the substrate (9). Similar considerations exist at interfaces formed by plasma and chemical oxidation of the Si substrate. Additionally, differences in linear thermal expansion coefficients between SiO_2 (~0.5 x 10^{-6} C^{-1}) and the Si substrate (~2.5 x 10^{-6} C^{-1}) contribute a component of thermal strain equivalent to several tenths of a percent for oxides grown, or processed at 800°C to 1000°C, and then returned to room temperature (10). These levels of interfacial bond-strain cannot be relieved elastically, and this pins a relatively high level of stress at the interface, ~5x10^9 dynes-cm^{-2}, and additionally produces bonding defects. In particular, these levels of interfacial stress result in *plastic deformation*, as indicated by the ion scattering measurements of (3), with Si dangling bond formation in the Si_D layer. Typical densities of dangling bonds as determined by electron spin resonance (ESR) are approximately 2-3x10^{12} cm^{-2} or on average about 0.3 % of the Si atoms at the surface of a crystal oriented in the <111> or <001> directions (10,11). The symmetry of the g-tensor establishes that these dangling bonds reside in the Si substrate, and the in-plane bonding of the Si atoms is locally in tensile stress at these defect sites as evidenced by the g-tensor. Defect formation is also consistent with a novel application of bond constraint theory (BCT), to semiconductor-dielectric, and internal dielectric interfaces as well (12, 13).

Bond constraint theory has provided important insights to the physical mechanisms underlying i) the formation of ITRs, and ii) defect formation and defect relaxation at these interfaces. Lucovsky, Phillips and coworkers have pointed out that Si-SiO_2 interfaces are heterostructures in which the substrate Si is effectively *rigid or over-constrained*. The ITR provides a continuous and smooth *transition* between tensile stress in the Si substrate and compressive stress in the SiO_2 dielectric. The bonding changes after the 900°C anneal can then be construed as a strain-driven self-organization that prevents percolation of in-plane rigidity and thereby provides a low defect and defect precursor layer that bridges the Si substrate to the SiO_2 dielectric. SXPS studies have indicated that in as-grown Si-SiO_2 interfaces the bonding in the ITR is random; however, after a 900°C anneal, the bonding is *non-random* with Si-rich and O-rich regions. Non-random bonding after the 900°C RTA encapsulates the Si-rich groups to prevent percolation of in-plane bond-strain. This self-organizing transition establishes the unique properties of the Si-SiO_2 interface including, low defect densities(10^{11} cm^{-2}), excellent reliability under electrical stress, and most importantly the universal mobility relationships for both holes and electrons (14,15). These electrical properties and the associated reliability have become the metrics for all future generations of gate dielectrics and their interfaces with Si.

In the second generation of scaling EOT, selective nitridation of SiO_2, and the Si-SiO_2 interface has been integrated into the manufacturing of CMOS devices with EOT values extending to ~1.1 to 1.2 nm. Studies of nitridation processes led to an important paradigm that extends to deposited high-k dielectrics (nanocrystalline and epitaxial transition metal, TM, and rare earth, RE, elemental and complex oxides with physical thicknesses > 3 nm), namely that the processing protocol must include separate and

independent steps for interface formation and the deposition of the dielectric film (15). The concept of separate and independent control of interface formation and thin film deposition has also lead to the identification of a nitrogen profile that optimizes performance and reliability of stacked devices with Si oxynitride alloy dielectrics, and to a processing route to realizing this profile (16, 17). Those processing steps, as elucidated by the Lucovsky group at NC State University, includes the formation of 0.6 nm of Si oxide including an SiO transition region by using remote plasma assisted oxidation at 300°C, followed by a remote plasma nitridation, also at 300°C, to insert one monolayer of N between SiO_x and Si. The SiO component of the interfacial oxide bridges tensile stress in Si substrate and compressive stress in oxide while the SiO_2 component removes positive fixed charge away from the transport channel. The monolayer of interfacial nitrogen: a) reduces interface stress gradient and thereby improves reliability and b) increases the conduction band offset and provides a 10-fold reduction in direct current. Just as the composition of the ITR varies between that of Si and SiO_2, the effective dielectric constant of the region would be expected to vary. Measurements have shown that the 0.6 nm physically thick layer has an EOT of about 0.3 nm. Annealing high k dielectrics and the interfacial layer in D_2 has also been shown to reduce oxide charge and interface states and to enhance channel mobility. An alternate approach to defect reduction involved compensation of defect sites using NH groups, which mimic O.

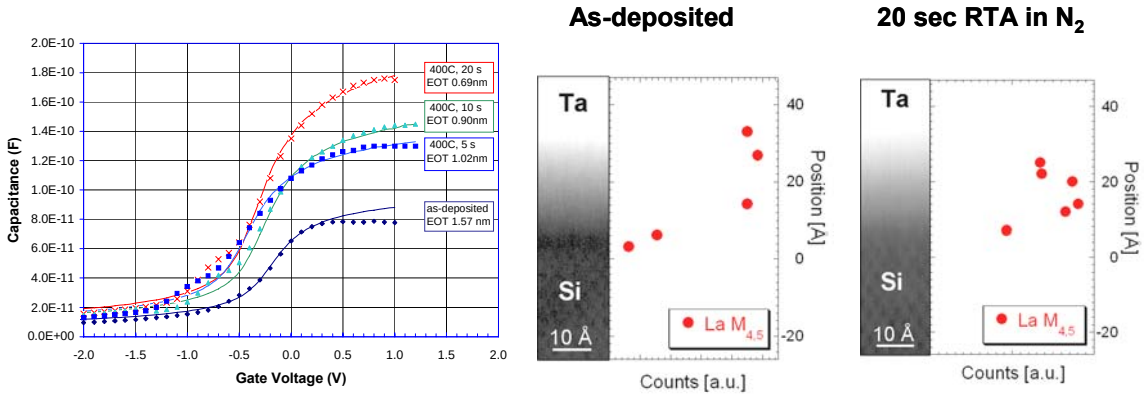
Reduced Interfacial Layers

Reduction of the EOT below about 0.7nm becomes additionally complicated. First of all, the interfacial layer, described above, starts to dominate the overall EOT and must be reduced. Second, a higher dielectric constant dielectric is desired to preserve a total film thickness of 2-3 nm so that atomic-level fluctuations do not adversely impact control of EOT, which is specified at 4% in the ITRS (18). Two strategies have emerged to reduce the effective thickness of the interfacial layer: a) reduce the thickness of a previously-formed ITR layer and b) eliminate the ITR layer by depositing the high k directly on Si. In the case of $LaAlO_3$, an amorphous film (to begin with) can be deposited; other materials require epitaxial deposition.

Reduction of a Grown Interfacial Layer. In this work La_2O_3 has been successfully used to reduce the effective thickness of the interfacial layer, through the reaction with SiO_2 to form La silicate. With this process EOT less than 0.5 nm can be produced. Figure 2 illustrates the reaction of a $W/Ta/La_2O_3/SiO_2$ stack showing a reduction in EOT from 1.57 to 0.69 nm after a 20 s 400°C RTA in N_2. The TEM pictures and EELS data show the consumption of the underlying SiO_2 to form a silicate layer.

Attempts to reduce or eliminate the interfacial layer have been thwarted by the unintentional growth of interfacial oxide, presumably via transport of oxygen from the capping layer, metal gate or even the annealing atmosphere through the high k dielectric layer, as seen in Fig. 3, where the EOT of a TaN/La_2O_3 stack increased from 0.62 nm to 1.12 nm after a 10 sec 100°C RTA. Unfortunately such anneals are needed for two reasons: For one, source/drain junctions, which are performed after the gate stack, require high temperature annealing to activate. For another, high temperature anneals are needed for interface relaxation to minimize interfacial strain and to reduce oxide charge and interface states, which in turn affect device performance and reliability. For the samples shown in Fig. 3 for example, the net effective charge was reduced by $5x10^{12}$ charges/cm^2

and the interface density was reduced by $5x10^{12}$ states/cm^2-eV. Without such annealing, the MOS properties of such dielectrics are not acceptable for high performance CMOS applications.



a) b)

Figure 2. Reduction of EOT by the reaction of La_2O_3 with SiO_2: a) as observed by CV measurements as the annealing time is increased, and b) as observed by High Resolution TEM, including electron energy loss, EELS, measurements

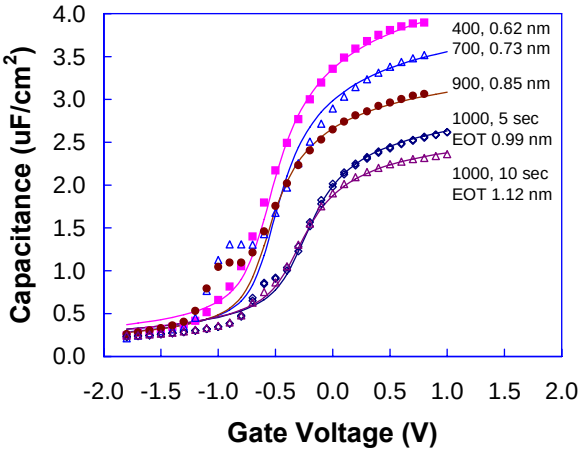


Figure 3. Increase in EOT of a TaN/La_2O_3 gate stack during RTA in N_2

Amorphous $LaAlO_3$ on Si. Electron spin resonance analysis of $LaAlO_3$ /Si (001) structures with 30-60 nm thick amorphous $LaAlO_3$ layers grown by molecular-beam deposition reveals the absence of an Si/SiO_2-type interface in terms of archetypal Si-dangling bond-type Si/SiO_2 interface defects (P_{b0}, P_{b1}). With no P_b-type defects observed, this state is found to persist during subsequent annealing (5 % O_2 + N_2 ambient) up to an annealing temperature, T_{an}, ~ 800°C, indicating a thermally stable and abrupt Si/$LaAlO_3$ interface. In the range T_{an} ~ 800– 860°C, however, a Si/SiO_2-type interface starts forming as evidenced by the appearance of P_{b0} defects and, with some delay in T_{an}, the EX center (an SiO_2 associated defect) attesting to significant structural/compositional modification. The peaking of the defect density vs. T_{an} curves indicates that the interlayer with SiO_x nature breaks up upon annealing at $T_{an} \geq 930$°C, possibly related to crystallization and possibly silicate formation. No $LaAlO_3$-specific point defects could be detected.

The dielectric properties of the stoichiometric amorphous $LaAlO_3$ thin films deposited on (100) silicon were determined through capacitance-voltage and current-voltage measurements. The electrical measurements indicate that the amorphous $LaAlO_3$ thin films have a dielectric constant, $k = 16 \pm 2$ (19). This is significantly lower than the $k = 24$ of crystalline $LaAlO_3$. The equivalent oxide thickness (EOT) values range between 0.98 nm and 1.55 nm for films with physical thicknesses of 4.5 to 7.5 nm, deposited on *n*-type silicon. The thermal stability of these films was investigated by high-resolution transmission electron microscopy (HRTEM), transmission infrared absorption spectroscopy (IRAS), x-ray diffraction (XRD), and secondary ion mass spectroscopy (SIMS). IRAS indicated that the as-deposited films contained <0.01 nm of SiO_2 at the interface between $LaAlO_3$ and Si. The films were annealed in an N_2 ambient by rapid thermal annealing at temperatures between 700°C and 1000°C. XRD studies show that the films remain amorphous after annealing at 700°C, although HRTEM shows the presence of structural order on a ~1 nm length scale even in the as-deposited films. At RTA temperatures around 1000°C, however, recrystallization is observed in Fig. 4. Around that same temperature, diffusion of Al and La into the substrate from the dielectric is observed in Fig. 5 (20). The addition of nitrogen to the $LaAlO_3$ is seen to reduce both crystallization (Fig. 4) and diffusion of Al and La into the substrate (Fig. 6).

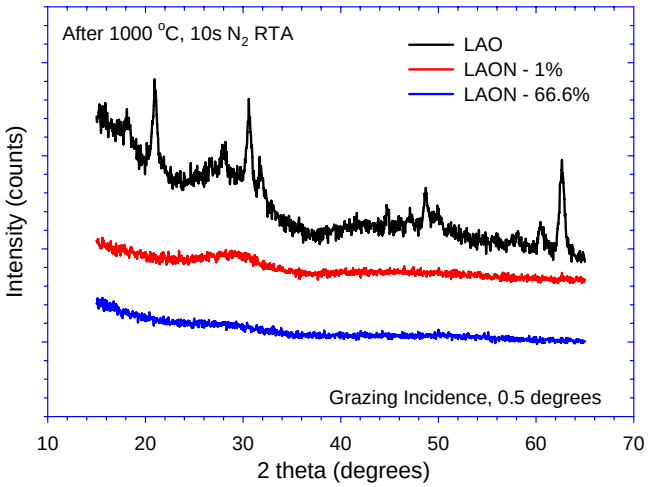


Figure 4. X-Ray diffraction patterns of $LaAlO_3$ and LaAl-Oxynitride films. The $LaAlO_3$ films are nanocrystalline at 1000°C, while nitrogen additions are seen to inhibit the crystallization seen by XRD peaks.

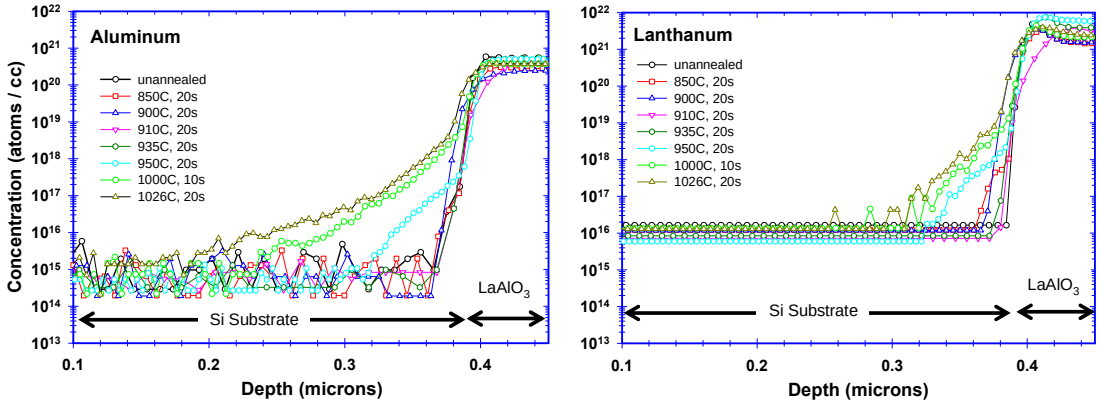


Figure 5. Backside SIMS showing diffusion of Al (left) and of La (right) from a $LaAlO_3$ film into the substrate after 20 s annealing at 950°C, after (20)

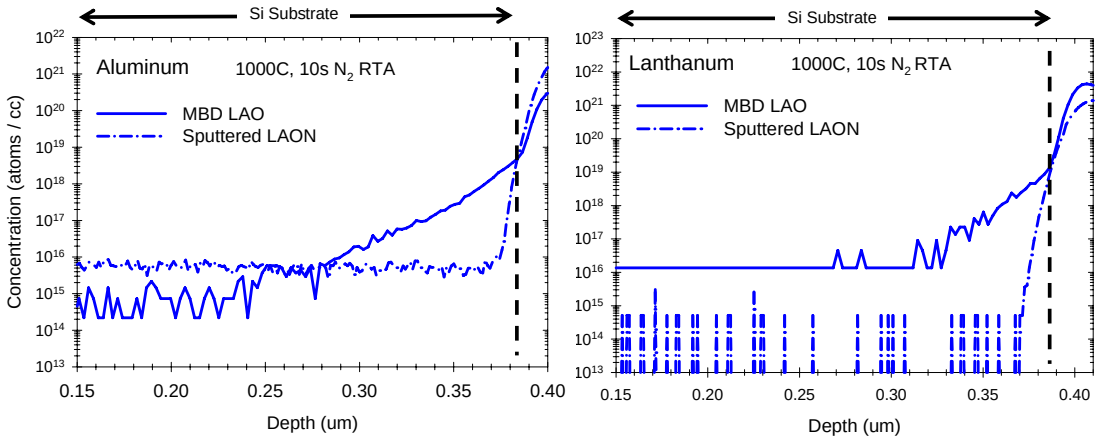
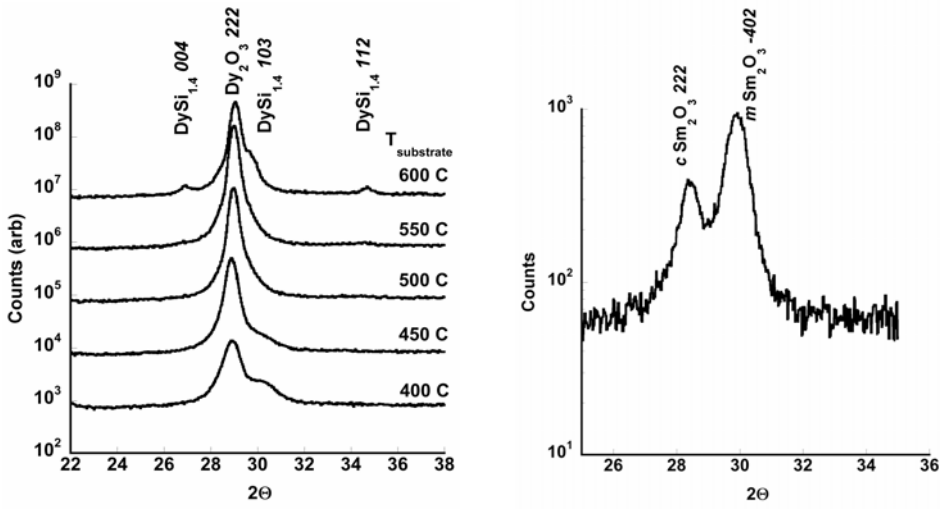


Figure 6. Backside SIMS showing the reduced diffusion of Al and La into the substrate in LaAlON films compared to $LaAlO_3$

Epitaxial Dielectrics. There are two fundamental interface issues with the use of epitaxial dielectrics on Si. First of all the (100) surface of Si is simply too reactive, and growth of a complex oxide, e.g., $SrTiO_3$ requires the formation of a SrSi interface, and the subsequent depositions of alternating planes of SrO and TiO_2. The SrSi interfacial layer generates large amounts of fixed charge, and rules out applications of the epitaxial films as gate dielectrics.

In contrast, it is possible to grow epitaxial complex oxides on Si(111) due its reduced reactivity. In our work, Sm_2O_3, Dy_2O_3 and Ho_2O_3 have all been deposited in an attempt to comprehensively evaluate the Lanthanide rare earth series of materials. A starting problem is that this epitaxial deposition must be done under very precisely controlled partial pressures of oxygen. Too low a pressure of oxidant (O_2 or O_3) leads to silicide formation, as seen with Dy in Fig. 7a, and the order of exposure of the substrate to oxidant and metal, i.e., oxidant first versus metal first, may play an important role in film formation and evolution. Mixing of multiple oxide phases is another problem, shown with Sm_2O_3 in Fig 7b.



a) b)

Figure 7. X-Ray diffraction patterns of deposited rare earth oxides, illustrating problems with epitaxial deposition on (111) Si: a) Dy_2O_3 films, showing the presence of silicide and b) Sm_2O_3 films, showing mixing of monoclinic and the desired cubic bixbyite phases

Unfortunately as these epitaxial films get thicker they are observed to roughen as they crystallize, leading to the second fundamental issue, namely that nano-crystalline oxides greater than ~3 nm have very high densities of (divacancy) defects at internal grain boundaries. These defects are typically charged to begin with or are sites for trapping of charge during device stressing. Such charge next to the channel dramatically reduces mobility. These have not as yet been researched sufficiently to make any judgments relative to CMOS applications. The main concern is that any reductions in EOT, may, in large part, be compensated by reductions in electron and hole channel mobilities.

Interface Between High k Dielectric and SiO_2

Based on the same bond constraint theory discussed earlier, a abrupt interface between a nanocrystalline, high-k elemental oxide and an SiON interfacial layer will generally have high densities of fixed charge, about one order of magnitude higher than those at SiO_2-optimized Si oxynitride ($(SiO_2)_{0.5}(Si_3N_4)_{0.5} = Si_2ON_2$) non-crystalline dielectrics, i.e., of the order of $2\text{-}5x10^{12}$ cm^{-2}. This high level of fixed charge at the SiON-nanocrystalline interfaces will degrade channel transport.

High k Dielectric

Within the FEP Research and Transition Centers, a myriad of binary and ternary oxides, silicates, aluminates, and nitrides were examined. Table I summarizes the materials studied as part of the SRC-SEMATECH Center for Front End Processing. The number of materials evaluated was even larger than the list suggests since many of the materials can be deposited by different techniques, and the microstructure, stoichiometry, interfacial layer to the Si, and the chemical purity of the material depend strongly on how the material was prepared. An additional compounding factor is the fact that nitrogen, which as earlier shown to improve the material stability and to retard the diffusion of Boron from a poly-Si gate, can be introduced in a number of different ways, each of which dramatically influences the material formed.

TABLE I. High k Dielectrics Studied.

Materials		**Other Parameters**
Ta_2O_5	Al_2O_3	Deposition Technique
	$Al_xSi_yO_z$	RTCVD
TiO_2		RPECVD
TiO_2/Si_3N_4	Y_2O_3	JVD
TiO_2/HfO_2	$Y_xSi_yO_z$	Sputtering (metals)
		MBD
ZrO_2	La_2O_3	ALD
$Zr_xSi_yO_z$	$La_xSi_yO_x$	MOCVD
$(ZrO_2)_x (SiO_2)_y (Si_3N_4)_z$	$LaAlO_3$	
$Zr_xTi_yO_z$		Nitridation
	Gd_2O_3 , Gd_2O_3/ HfO_2	
HfO_2	Dy_2O_3 , Tb_2O_3	N Incorporation
$Hf_xSi_yO_z$ (+N)	Sm_2O_3 , Pr_2O_3	Alloy with Si_3N_4
$(HfO_2)_x (SiO_2)_y (Si_3N_4)_z$	Yb_2O_3 , Lu_2O_3	Anneal (N_2, NH_3)
$Hf_xTi_yO_z$		Plasma
$Hf_xAl_yO_z$	$Sr_xHf_yO_z$	
	$LaScO_3$	
CeO_2	$GdScO_3$	
	$DyScO_3$	

Nanocrystallation, Point Defects, and Electronic Energy Levels in High k Materials

HRTEM Studies. The high electronic polarizability needed to have a dielectric constant higher than 10, i.e., in materials other than SiO_2, Al_2O_3, and Si_3N_4, comes from ionic bonding. With very few exceptions, this same ionic bonding means that the stable form of the material is in the (nano) crystalline state. Indeed, with very few exceptions, in all the materials we have studied (Table I), nanocrystallization is observed after annealing at 1000°C, i.e., junction annealing temperatures. The grain sizes may be too small to be seen with some techniques, e.g., XRD, but invariably careful HRTEM and spectroscopy invariably detects the nanocrystallization. Figure 8 provides HRTEM images of this nano-crystallization in a number of materials after annealing. In contrast to HfO_2 and $LaAlO_3$, where nanocrystallites are seen, the grains of $HfTiO_4$ are very large.

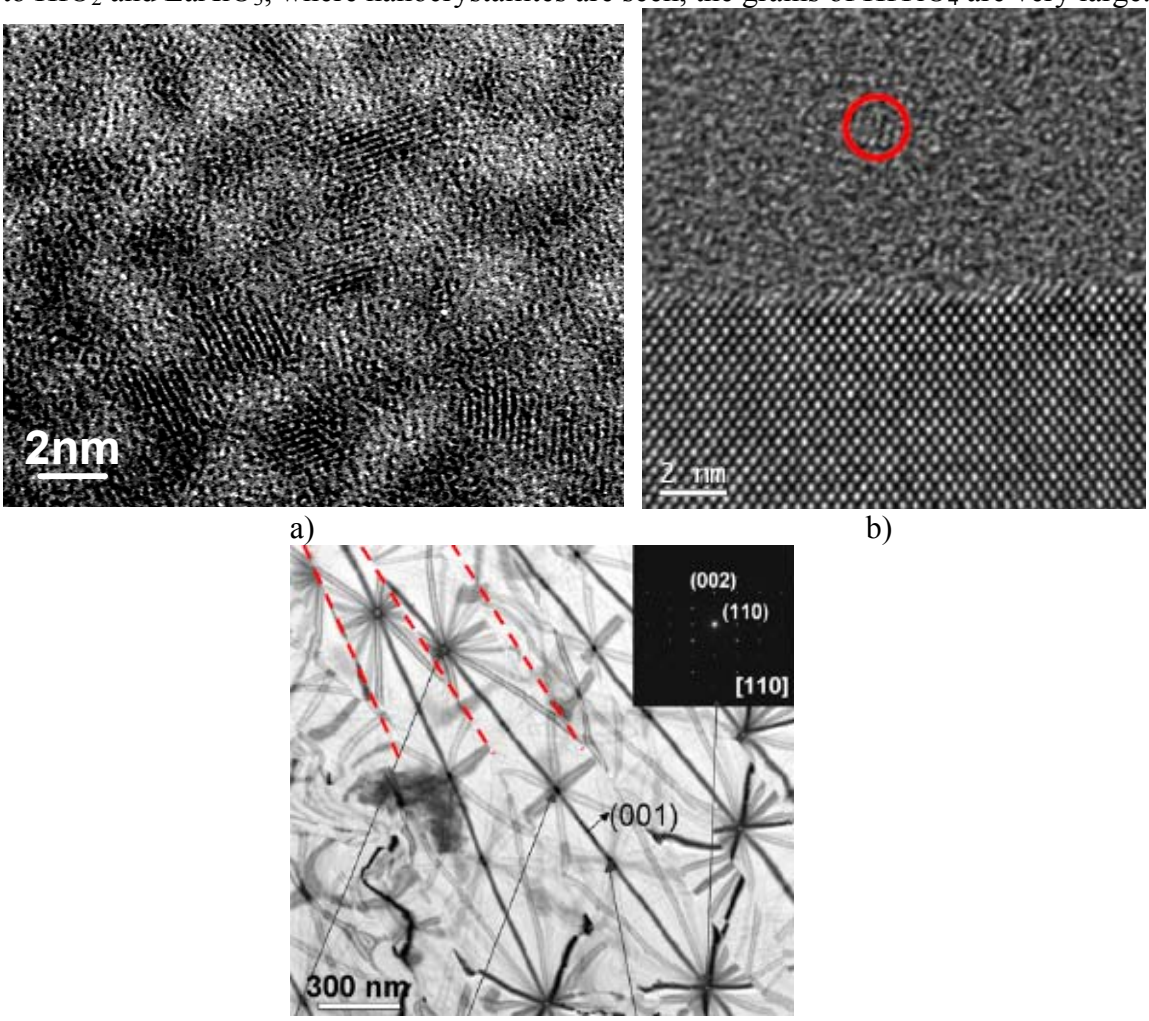


Figure 8. Crystallization as seen by HRTEM in: a) 8 nm Hf-silicate film with 60 mol% SiO_2 after rapid thermal annealing at 1000°C for 10 s (image recorded by Yan Yang (UCSB); sample supplied by P. Lysaght (SEMATECH)), b) $LaAlO_3$ annealed for 20 s at 850°C, c) 35 nm thick $HfTiO_4$ where the dashed lines indicate the location of some grain boundaries. (the "spiders" are bend contours due to the buckling of the film to relieve the larger thermal mismatch stress. Electron diffraction confirmed that the film was orthorhombic $HfTiO_4$ (21))

Spectroscopy Studies. A major consequence of the nanocrystallization is the presence of point defects, e.g., vacancies and interstitials, which have electronic energies within the bandgap of the dielectric. As with all such states, depending on the position of the Fermi level with respect to the state energy, they can be positive, neutral, and negative, and they can dynamically trap or detrap charge. In the charged state they can shift device threshold voltages and degrade mobility, and in the trapping mode they can lead to time-dependent shifts in device characteristics. In addition, states whose energy is a few tenths of an electron volt below the conduction band of the dielectric result in high gate leakage currents, either via a bandgap narrowing of the dielectric or via trap-assisted-tunneling through the states.

Of particular interest in our studies have been two different electrical defects previously identified by the IMEC group through J-V and C-V studies: i) traps near the conduction band edge of HfO_2 that contribute to temperature-dependent trap assisted tunneling (TAT) and Frenkel-Poole (F-P) conduction under conditions which permit injection of electrons from n-type substrates (with a positive gate bias) through composite gate stacks that include SiO_2 interfacial layers and HfO_2 dielectric films (22, 23), and ii) other traps in the HfO_2 band gap that are below the conduction band edge of the substrate Si band gap and detected by substrate injection of holes for a negative gate bias (22, 23). The markedly different electron and hole trapping properties of these intrinsic defects are a potentially serious problem for threshold voltage control and stability in CMOS inverter FETs using nanocrystalline $Hf(Zr)O_2$ dielectrics. The IMEC group has estimated an electron trap depth of about 0.5 to 0.8 eV, whereas similar trapping has also be reported by the SEMATECH group with an estimated trap depth of ~0.3 to 0.4 eV relative the conduction of HfO_2 (24). Based on frequency dispersion in C-V plots, the IMEC group has estimated that the hole trap is ~0.3 eV below the conduction band edge of Si, and that this trap is correlated with Hf-O bonding in the immediate vicinity of the Si substrate.

There have been recent theoretical calculations by the Robertson group (25) and Foster group (26, 27)that have addressed the energies of O-vacancy defects with the forbidden gaps of ZrO_2 and HfO_2. These calculations give somewhat different results. The experimental results of our group reported in this paper, and the IMEC results in (22, 23), suggest that both defects are in the upper half of the respective TM oxide band gaps. Our results and the IMEC/SEMATECH results will be combined in an empirical model for the defect state energies of the neutral and negatively charged O-atom vacancies. This approach is consistent with the results of (25), where it was suggested that differences between the calculated defect state energies in (25), and (26, 27) was associated at least in part with an underestimate of conduction band energies/empty state energies that is inherent in the DFT/LDA calculations of (26,27).

Spectroscopic techniques, e.g., vacuum ultra-violet spectroscopic ellipsometry (VUV SE) and near edge x-ray absorption (NEXAS), provide a good way to more directly observe the energy level (crystal field) splittings that occur when the dielectric crystallizes. As such, spectroscopy, along with HRTEM, has proven to be a most sensitive measure of nanocrystallization. Furthermore, Spectroscopic studies have revealed features that are not part of the fundamental electronic structure of both HfO_2 and ZrO_2 (28). Work in the Center, supported by theory indicate that neutral and negatively charged O-atom vacancies are the most important intrinsic defects in nanocrystalline thin films of $Hf(Zr)O_2$. O-vacancy defects are active as i) interface traps

for Si substrate injection of holes, and ii) bulk film traps for Si substrate injection of electrons. Figure 9(a) displays the O K_1 spectrum for ZrO_2. Figure 9(b) is a Gaussian fit to $4d_{3/2}$ (E_g) and $4d_{5/2}$ (T_{2g}) d-state features in the O K_1 spectrum for ZrO_2. The degeneracies of these states have been completely removed by the Jahn-Teller bonding distortions attributed to departures from a cubic CaF_2 structure. Figure 9(c) is a blow-up of the spectrum in Fig. 9(b) that identifies the feature that has been assigned to the O-vacancy (28). A composition range has been found where O-vacancy defects are not observed spectroscopically in thermally and chemically stable Zr Si oxynitride alloy films, $(SiO_2)_x(Si_3N_4)_y(ZrO_2)_z$, that have been annealed at 1100ºC in Ar. However, the Si_3N_4 concentrations in these alloys must be controlled within narrow limits, ~0.36 to 0.4, with equal SiO_2 and ZrO_2 concentrations of approximately 0.32 to 0.3.

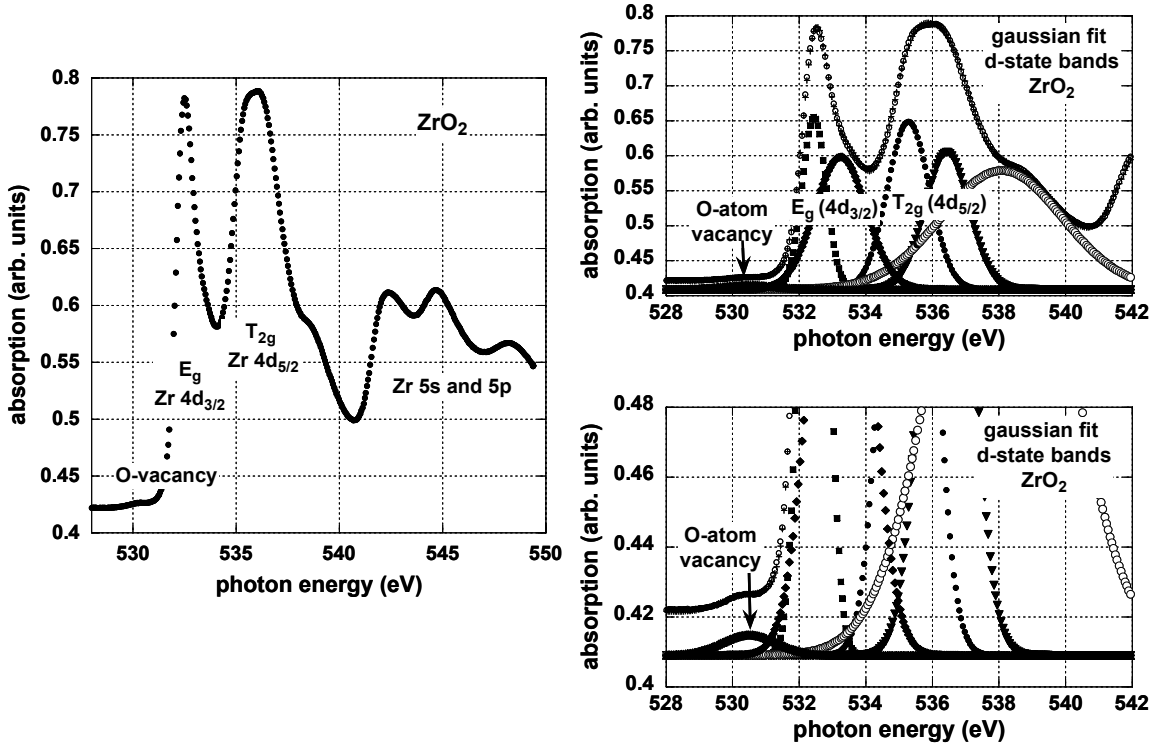


Figure 9. O K_1 edge spectra of ZrO_2 annealed to 900°C: a) absorption spectrum displaying Zr 4p, 5s and 5p, and O-atom vacancy features, b) Gaussian fit to 4d state features, and c) expanded Gaussian fit to display O-atom vacancy

Another adverse effect of nanocrystallization is the enhancement in diffusion of metals through the dielectric and into the substrate. As seen earlier, in Figs. 4-6, the onset of La and Al diffusion into the substrate from $LaAlO_3$ correlates strongly with the crystallization temperature of the film. The addition of nitrogen into the film, by sputtering in N_2 + Ar, where the flow ratio $N_2/(N_2 + Ar)$ = 66%, delays the onset of both crystallization and diffusion into the substrate. These results are therefore consistent with the improvement of the gate stack thermal stability from an impurity diffusion point of view, where the film morphology is controlled to avoid grain boundary formation (29).

Electrical Characterization of Traps and Trapping-related Instabilities. Inelastic Electronic Tunneling Spectroscopy, IETS, is proving to be a powerful technique for probing the microstructure, impurities, and traps in ultra-thin gate dielectrics, and we have used it to learn a lot about high-k gate dielectrics (30-32). Figure 10 shows an IETS

spectrum of a HfO_2 film on Si, where features for the HfO_2 phonons, Si phonons, and Si-O bonding vibrations have been identified. Figure 11 shows that, by measuring the IETS signals for both polarities, one can probe the microstructures near both the HfO_2/Si interface and the gate electrode/HfO_2 interface. Figure 12 shows the generation and evolution of traps caused by voltage stress. Figure 13 shows that the trap features are revealed in the IETS spectra for both polarities, and the voltages at which the pair of trap features occurs allow the determination of the energy and location of the trap.

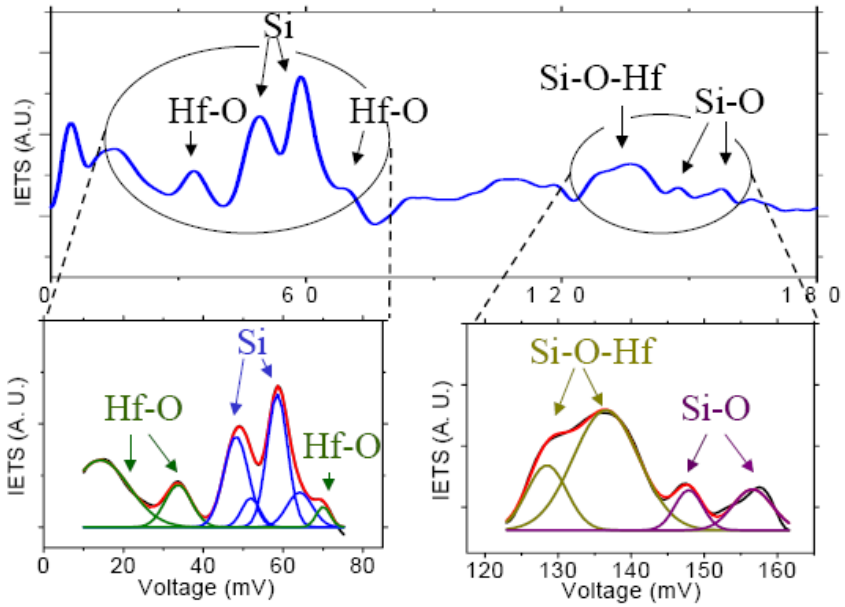


Figure 10. IETS spectrum of HfO_2 on Si, showing features for Si phonons, Hf oxide phonons, Si-O-Hf vibrations, and Si-O vibrations

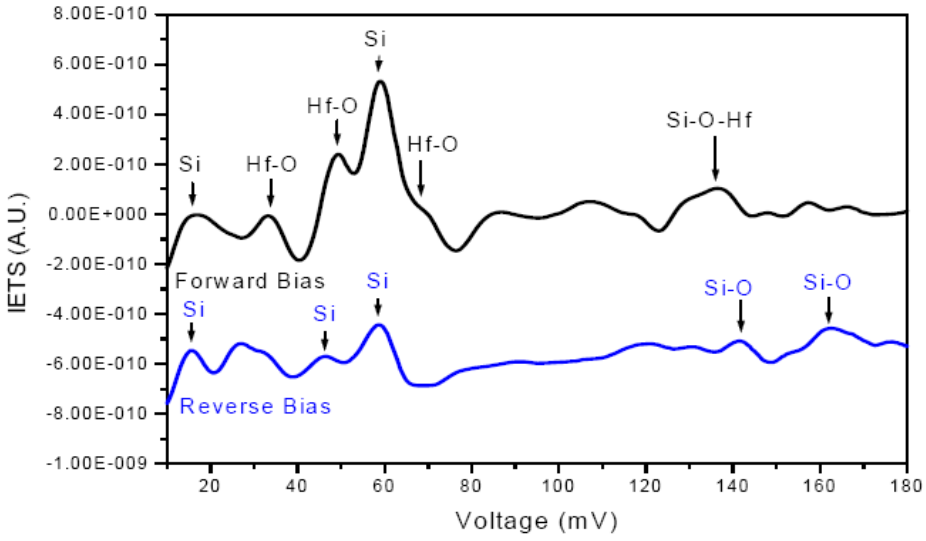


Figure 11. IETS spectra for the same sample as in Fig. 10 measured at two different polarities, revealing Si-O bonding vibration near the Si interface and no such bonding near the gate electrode interface.

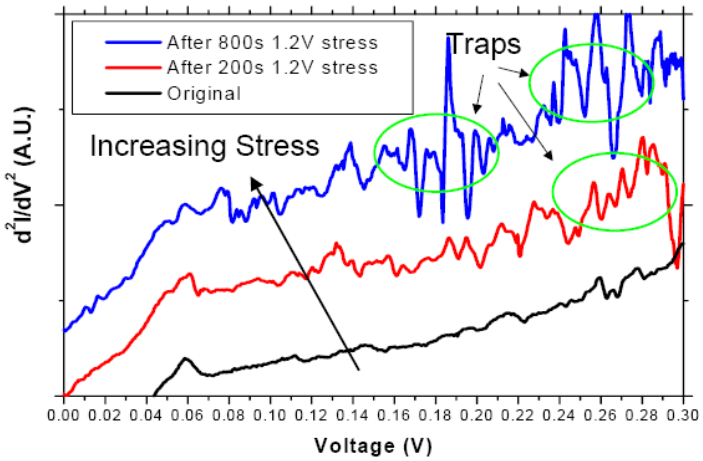


Figure 12. Trap features appearing in EITS spectrum of HfO_2 after electrical stress

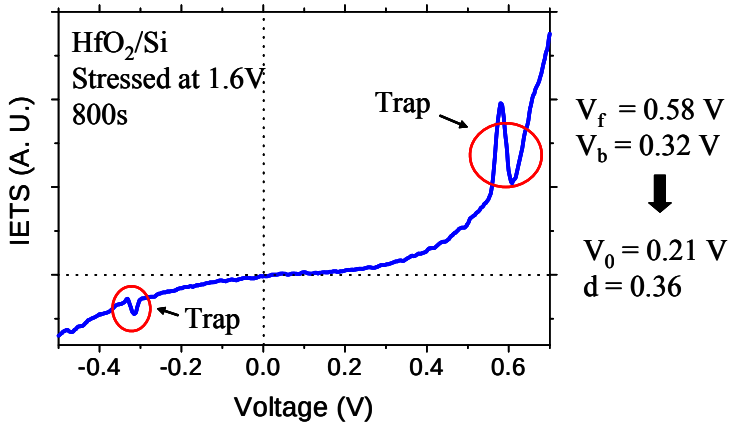


Figure 13. Trap features that appear in pairs allow determination of the trap energy and the trap location. Here the EOT of the dielectric is ~ 2.5 nm and the trap is located 0.9 nm from the dielectric/Si interface.

Electrical characterization of high k dielectrics needs to consider the effects of trapping for proper understanding of the results. For example, in the process of studying HfO_2-based MOSFET characteristics, we realized that, because of significant trapping of carriers, the channel "mobility" extracted by the conventional method is grossly inaccurate. Therefore, we developed a methodology to correctly extract the channel mobility in the presence of trapping (33, 34), which has contributed significantly to our understanding of the mobility degradation phenomenon frequently observed in high-k gated MOSFETs. Figure 14 shows that the corrected mobility is substantially higher than the mobility extracted by the conventional method, which does not take into account the trapping effect. Figure 15 shows that the mobility decreases systematically with increasing density of interface traps, suggesting that Coulomb scattering is a major factor for mobility degradation. Using these corrections we have been able to extract the temperature dependence of the mobility—in particular, the temperature dependence of the phonon-limited mobility, as obtained by subtracting the Coulomb component and the surface roughness component from the measured effective mobility over a range of temperatures. These results indicate that the phonon limited mobility for high-k gated MOSFET is lower than that of the SiO_2-gated control, suggesting that the high-k gated MOSFET sufferers from an additional phonon scattering mechanism, most likely from the phonons of the HfO_2 layer.

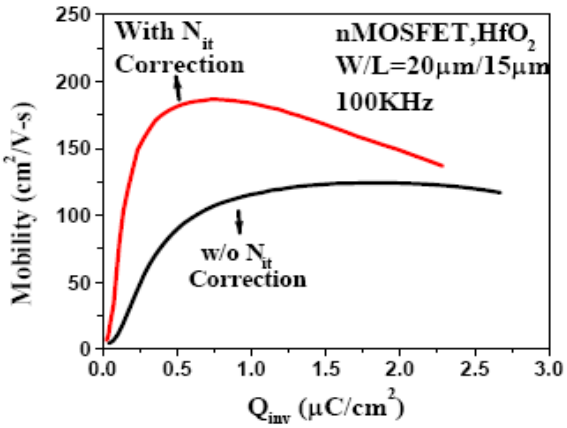


Figure 14. Extracted channel mobility using conventional methods (bottom curve) versus the new method with N_{it} correction (top curve)

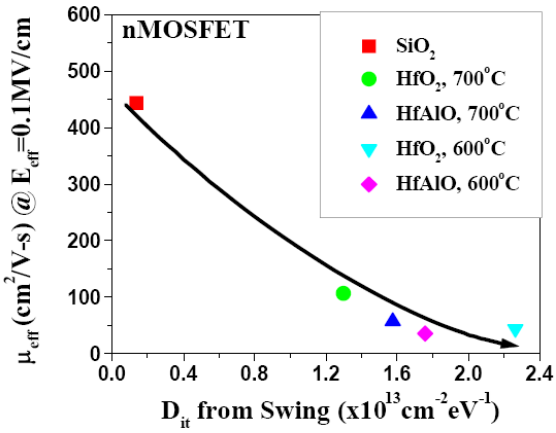


Figure 15. Systematic degradation in the effective mobility with increases in the interface trap density

Hf(Zr) Family of Materials

The leading candidate for ≥ 0.7nm EOT applications continues to be the Hf(Zr) family of materials. The ITRS gate leakage requirements are met with these films. Optimization of the material and integration process, to reduce charge in the dielectric, results in high channel mobility. Representative results for a 1 nm EOT material includes: > 90% of oxide mobility, N_{it} of 5 x 10^{10}/cm^2, N_f of 4 x 10^{11}, hysteresis < 30 mV, and a ten-year ΔV_t < 30 mV. Measurements made within and outside the Center confirm that reducing the thickness of the dielectric can dramatically enhance its stability against charging.

Detection and Presence of Hf in SiO_2-like Interfacial Layers. Using STEM/HAADF, stacks with HfO_2 dielectric films from two different collaborators (SEMATECH and Philips/IMEC/Motorola) showed interfacial roughness at the SiO_2/HfO_2 interface and the presence of Hf-clusters. Figure 16 shows (a) an HAADF image of the stack with the HfO_2 on chemical SiO_2 and confirms that the probe size is less than 0.2nm by resolving the Si dumbbells as shown from (b) the line intensity profile. The Si/SiO_2 interface appears rough when the brightness and contrast of the image was adjusted to define where the Si lattice ends. Furthermore, the image shows some bright intensity within the interfacial layer indicating the presence of heavy Hf atoms (inset). The non-uniform

intensity within the layer could be due to the variation in depth locations of the Hf clusters. The line intensity profile (b) shows that the Hf atom(s) are only ~ 0.5nm away from the interface. No Hf was detected in the SiO_2 layer interior or near the interface with Si. However, roughness caused the effective thickness of chemically pure interfacial SiO_2 to be thinner than it appears in conventional HRTEM images, which are less chemically sensitive, i.e., the "pure SiO_2" layer thickness can be as low as ~ 0.5nm, although in HRTEM, the thickness appeared to be ~ 1 nm.

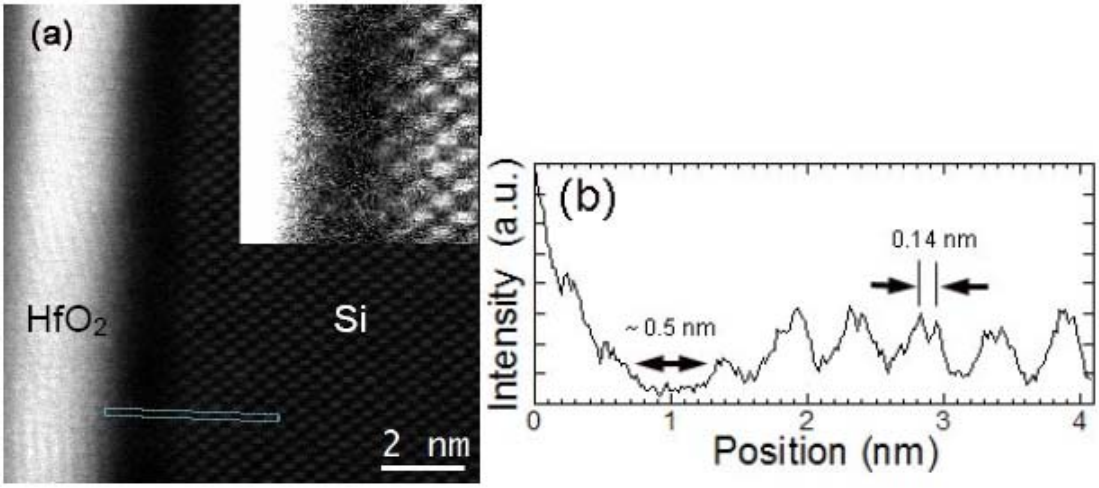


Figure 16. High-resolution HAADF image of HfO_2 grown on a chemical oxide and the location of the line intensity profile shown in (b). The inset is a magnified image of the interfacial layer

Trapping and Reliability of Hf-based Dielectrics. The PASHEI (Pulse Agitated Substrate Hot Electron Injection) technique has been used to determine trapping in Hf-based dielectrics. This technique has the advantages of the substrate hot electron injection technique (i.e., the ability to independently control the injection field and the gate field) without the need for an additional PN junction emitter. Figure 17 shows the threshold voltage shift as a function of the injected electron fluence, for a TaSiN/HfO_2/p_Si gate stack, from which the trap characteristics (density and capture cross-section) have been calculated.

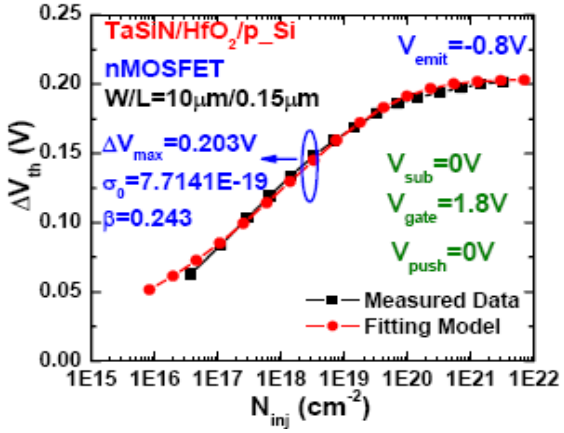


Figure 17. Threshold voltage as a function of the number of injected electrons. Such a curve allows determination of such trap parameters as trap density, N_t, capture cross section, σ_0, and distribution width, β, using $\Delta V_{th} = (qN_t/C_{ox})\{1 - \exp(-(N_{inj} \bullet \sigma_0)^{\beta})\}$ (35).

Carrier separation measurements, in which the gate, substrate, and channel current are simultaneously measured to determine the charge carrier(s), show that in NMOSFETs electrons from the inversion channel are predominantly injected into the gate stack. Capacitance voltage characteristics show a frequency dependence of the capacitance, reflecting trapping (Fig. 18a), and gate leakage measurements as a function of temperature, in Fig. 18b, show a pronounced dependence on temperature—consistent with Frenkel-Poole conduction or trap-assisted tunneling—providing further evidence of the shallow trap states below the HfO_2 conduction band, as discussed earlier. More careful examination of literature photoconductivity data (36, for example), reveals a considerable contribution of band edge, defect states to the leakage current.

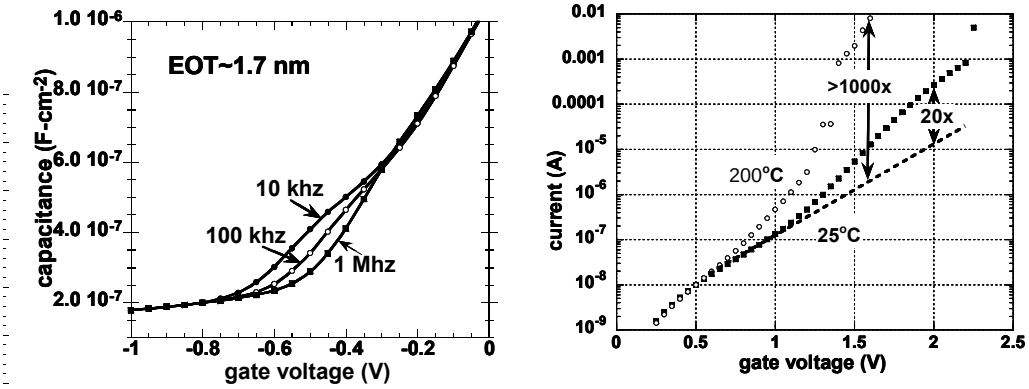


Figure 18. Characterization of a 1.7 nm EOT, SiO_2 (0.6 nm)/HfO_2 gate stack showing: a) frequency dependent CV curves, and b) temperature dependent gate leakage consistent with Frenkel-Poole conduction or trap-assisted tunneling

As part of the reliability assessment of HfO_2 based high-k gate dielectrics, we concluded that charge trapping poses much more of a threat to the operating lifetime than TDDB (37, 38). Figure 19 shows a typical example that supports the above statement, where one can clearly see that the charge trapping-induced threshold shift imposes a much more severe restriction on the maximum operating voltage than that deduced from TDDB (1.14V *vs* 2.9V in this example). Since then, we focused our reliability study on charge trapping effects, and have found the following general trend, at least in the numerous samples that we have studied: charge trapping is much more severe in poly-Si gated MOSFET's than that in metal gated MOSFETs (see Fig. 19a for an example).

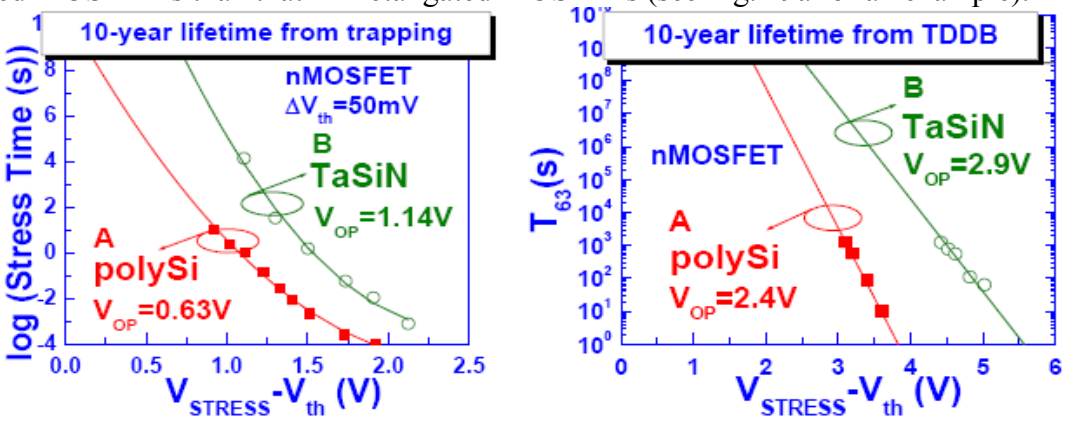


Figure 19. a) Trapping-induced threshold voltage shift imposes an upper limit for the operating voltage (0.63 V for poly-Si gate and 1.14V for TaSiN gate); (b) Time-Dependent Dielectric Breakdown (TDDB) limits the operating voltage at a higher value (2.4 V for poly-Si gate and 2.9 V for TaSiN gate)

Higher k Materials

As discussed earlier, the need to keep reducing EOT for every new generation of devices drives us both to reduce the thickness of the interfacial layer and to increase the dielectric constant of the high k. As hinted in Fig. 1, it is desirable that the high k layer be at least 5-10 atomic layers thick in order to meet the ITRS thickness control requirement (±4% 3σ). Earlier, the approach of reducing the interfacial layer was discussed. However, since the ITRS still envisions (hopes) that 0.4 nm EOT may someday be achievable, even without an interfacial layer materials having higher dielectric constants than HfO_2 may ultimately be needed. If an interfacial layer is proven to be necessary in the long run, even higher k materials will be required. Two approaches to achieving higher k have been examined: one is to start with the Hf-based dielectric and to modestly increase the effective dielectric constant through layering or alloying HfO_2 with higher k materials; the second is to employ even higher k, usually ternary, dielectrics either in an amorphous state or as an epitaxial film. Despite the seemingly overwhelming obstacles to this second approach, the potential rewards to a new breakthrough are great.

Layered and Alloyed Hf-based Dielectrics. We have studied laminates, e.g. HfO_2/TiO_2 (0.6 nm EOT achieved) or HfO_2/Gd_2O_3, as well as alloys, e.g., Hf-Sr-O, to further reduce EOT.

Titanium oxide was one of the early materials evaluated for high k applications; although it has a very high dielectric constant, it was abandoned because of its low barrier height. However, when sandwiched between layers of HfO_2, we have found it is possible to increase the effective dielectric constant of the stack without incurring too much of a penalty in increased leakage current. Both layers showed negligible intermixing and no silicide formation. For the first time, ultrathin EOT (~0.8 nm) was achieved with increased permittivity (~36). Leakage current was slightly higher than with pure HfO_2 due to lower band offset of TiO_2. However, superior thermal stability (>950°C), significantly reduced hysteresis characteristic (~35mV), and comparable interface state density (~$10^{11}eV^{-1}cm^{-2}$) represented the high quality of this dielectric. Also, excellent subthreshold swing (~69mV/decade), increased transconductance, better current drive, and ~25% improved channel electron mobility compared to HfO_2 samples demonstrate the feasibility of application for future CMOS technology, see Fig 20.

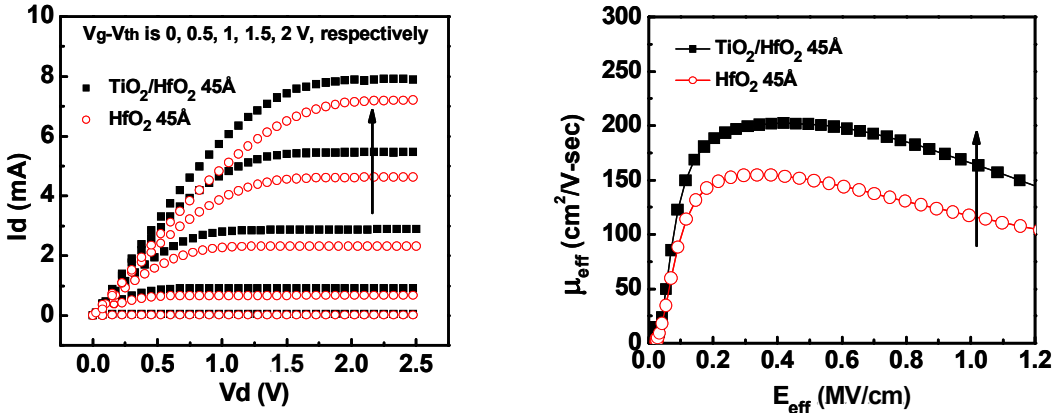


Figure 20. Comparison of NMOS devices having multi-layer TiO_2/HfO_2 dielectric of the same physical thickness (4.5 nm) as HfO_2: left) current drive; right) low field effective channel mobility

Even without the benefit of a higher k laminated layer, similar results have been observed with Gd_2O_3 on top of HfO_2, with an even greater mobility increase (60%). Figure 21 shows higher current drive, transconductance, and mobility in this system. Because of the complexity of high k systems, additional work is needed to fully understand these benefits, i.e., to what extent are they due to an improved interface versus a better high k dielectric.

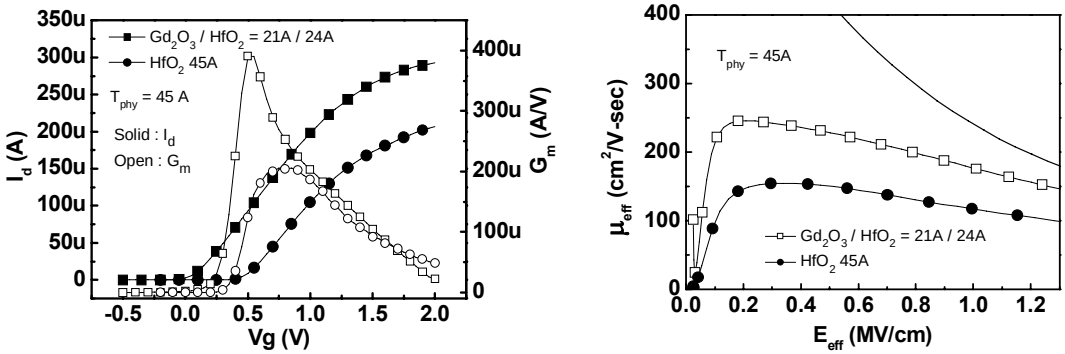


Figure 21. Comparison of NMOS devices having multi-layer $TaN/Gd_2O_3/HfO_2$ /p_Si of the same physical thickness (4.5 nm) as HfO_2: left) channel current and transconductance; right) low field effective channel mobility

Epitaxial and Amorphous Dielectrics. Molecular beam methods, in which the precise amount of oxygen can be controlled during growth, avoiding excess interfacial oxide layers, are preferred for epitaxial dielectrics—as least in the research phase. Medium energy ion scattering (MEIS) combined with temperature programmed desorption spectroscopy (TDS) and atomic force microscopy (AFM) has been used to study the interface composition and thermal stability of several epitaxial structures, including strontium titanate (STO) thin films grown on Si (001). The composition of the interface between the STO film and the substrate was found to be very sensitive to the recrystallization temperature used during growth, varying from a strontium silicate phase when the recrystallization temperature is low to a Ti–rich phase for higher recrystallization temperatures. The films are stable during vacuum annealing up to ~550°C, where SrO desorption begins and the initially flat film starts to roughen. Significant film disintegration occurs at 850°C, and is accompanied by SiO and SrO desorption, pinhole formation, and finally titanium diffusion into the silicon bulk forming a titanium silicide.

Metal Gate Electrodes

The continued scaling of CMOS devices beyond 45nm printed gate length requires the gate dielectric to have an EOT of 0.6 nm in these devices. The existing SiO_2 gate dielectric suffers from severe gate leakage in this regime and therefore, needs to be replaced by a high k material. For high performance devices, poly-Si gate electrodes have been reported to be incompatible with high k gate dielectrics because of depletion in the Poly-Si and because of Fermi level pinning of the gate workfunction (39, 40). Therefore, metal gate electrodes need to be integrated with the high k gate dielectrics in advanced CMOS devices. Just as with high k's, a considerable number of materials for this metal gate were examined in this center, as shown in Table II. Each of these materials, in turn,

could be deposited by a number of techniques. Finally, the capping layer on top of the metal gate electrode was shown to have a pronounced effect on both the EOT of the gate stack and the effective gate workfunction. While the requirements for high k dielectric are pretty much the same for all device applications, the metal gate workfunction requirements depend on the device technology, as detailed in Table III. The most stringent requirements for metal gate electrodes are for high performance bulk CMOS devices which need dual, band-edge metal gates. Low operating power devices made on fully-depleted SOI or with multi-gates (FINFET) need mid-gap workfunctions. Other applications require dual workfunctions that are slightly above and below mid-gap.

TABLE II. Metal Gate Electrodes Studied.

Materials		Other Parameters
Controls : Al, Poly-Si	Midgap	Capping Layers
	Silicides	W
Low ϕ :	TiN, AlN, WN	Poly-Si
Ta, TaN, Ta-Si-N, Ta-C		W/TaN
TaCN, TaSi(C)N	Tunable Alloys	
	Mo-Ta	Deposition
High ϕ :	Al-Ta (low ϕ)	PVD (conditions)
Noble Metals	Ru-Mo	ALD
Ru, RuO_2	Re-Ru (high ϕ)	CVD
Pt, Rh, Re, Ir		
Re-Ru	N-Implanted Mo	
Mo, MoN, Mo(C)N,	Simulation	
Mo(C)SiN	Zr	
Ta(monolayer)W	Mo	

TABLE III. Metal Gate Workfunction Requirements (According to 1005 ITRS)

Technology	High Peformance	Low Operating Power	Low Standby Power
Bulk CMOS	Dual Metal*: ~100 meV below E_C plus ~ 100 meV above E_V		
Single Gate (FDSOI)	Dual Metal*: ~150 meV above midgap ~150 meV below midgap	Midgap	Dual Metal*: ~100 meV below midgap ~100 meV above midgap
Dual and Multi-Gate (FinFET)	Midgap	Midgap	Dual Metal: ~100 meV below midgap ~100 meV above midgap

*Dual Metal workfunctions are for NMOS and PMOS, respectively

Effective Workfunctions of Metals on HfO_2

While, the effective workfunction of many candidate metal gates have been investigated on SiO_2 gate dielectric, their effective workfunction on high k gate dielectrics is under scrutiny. Recent reports have shown that the high work function metal gates suffer from a significant reduction in the effective work function on ultra-thin HfO_2 after subsequent anneals, which poses a challenge for the development of candidate metal gates suitable for PMOS applications (41-42). Furthermore, it has been demonstrated that the starting surface condition of HfO_2 before the metal gate deposition and the oxygen content at metal/HfO_2 interface play an important role in governing the effective work function of high work function metals (43). In light of this, our work tried to help understand the various factors that can affect the effective workfunction of metal gates on high-κ gate dielectrics. Accordingly, we learned that control of the metal gate workfunction requires control of a large number of process and material parameters, including the high k dielectric, the interface with the metal, the metal material, oxygen in

the deposited gate metal, and the capping layer on top of the metal. Oxygen at the metal-dielectric interface, where it can oxidize the gate metal and create oxygen vacancies, can greatly modulate the effective workfunction. Bonding of PMOS metals can lead to oxygen vacancies and Hf-rich interfaces, resulting in a workfunction change. In addition, the reaction of oxygen from the high k with the metal affects the charge levels present in the bulk of the high k. With Ru electrodes, not only does the effective workfunction vary with annealing, but the charge in the dielectric also varies. Interfacial layers under the HfO_2 can block oxygen vacancies and thereby impact the effective metal workfunction.

Effective workfunctions were electrically extracted by using the Hauser CV analysis to determine EOT and V_{FB} (44) of a series of MOS structures having varying thickness of both the interfacial layer and the high k dielectric (45). Figure 22 provides a plot of V_{FB} versus EOT after a 400°C, 30 min forming gas anneal (FGA), of a number of different metal and alloy gates on MOCVD HfO_2. In this experiment, the thickness of the high k layer was varied; it should be noted that there are various pros and cons about varying the interfacial layer, the high k layer, or both, and readers are referred to (45) for more discussion. Table IV compares the measured workfunctions with those on SiO_2. Unlike the case with Poly-Si gates, the effective workfunction of metal gates on HfO_2 is seen to vary, albeit not as much as for gates on SiO_2.

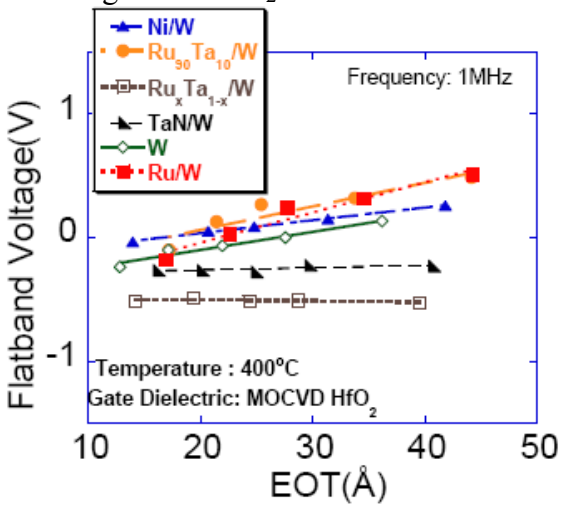


Figure 22. Flatband voltage versus EOT at 1 MHz after FGA on different metals on MOCVD HfO_2

TABLE IV. Workfunction of Metal Gates after FGA on MOCVD HfO_2*

Metal	ϕm (eV) on HfO_2	ϕm (eV) on SiO_2
W	4.67±0.02	4.7
Ru_xTa_{1-x}/W	4.5±0.03	4.5
TaN/W	4.72±0.03	X
Ni/W	4.88±0.03	4.8
Ru/W	4.67±0.03	5.1
$Ru_{90}Ta_{10}$/W	4.82±0.02	4.9

* Charge density at interfacial layer/Si interface was $8.64x10^{11} \pm 8.64x10^{11}/cm^2$

Interrelationship Between Workfunction and Charge. In order to study the implications of dipole modulation on the device properties, capacitance – voltage curves of MOS capacitors with Ru metal gate on HfO_2 gate dielectrics were measured. Figure 23 shows V_{FB} vs. EOT for these capacitors as-deposited and after anneals. A high effective work function ($\Phi_{m,eff}$) of Ru in the as-deposited state was observed from the intercept on

the V_{FB} axis. However, the $\Phi_{m,eff}$ of Ru reduced significantly after anneal, accompanied by a change in the charge profile at the HfO_2/IL/Si interface. The high $\Phi_{m,eff}$ of Ru in the as-deposited state can be attributed to Ru-O charge transfer and subsequent dipole creation at metal/HfO_2 interface which resulted in a high $\Phi_{m,eff}$. However, it is also believed that oxygen from Ru/HfO_2 interface moves towards HfO_2/IL/Si interface after anneal and manifest itself in the form of negative charges as can be seen from the positive slope of V_{FB} vs. EOT plots after anneal. The movement of oxygen from the Ru/HfO_2 interface to the HfO_2/IL/Si interface can allow Ru-Hf or Ru-Vo charge transfer at the Ru/HfO_2 interface which resulted in a lower $\Phi_{m,eff}$ (42). Therefore, in order to retain a high $\Phi_{m,eff}$ of PMOS metals on HfO_2, it is important to stop the movement of oxygen from metal/HfO_2 interface.

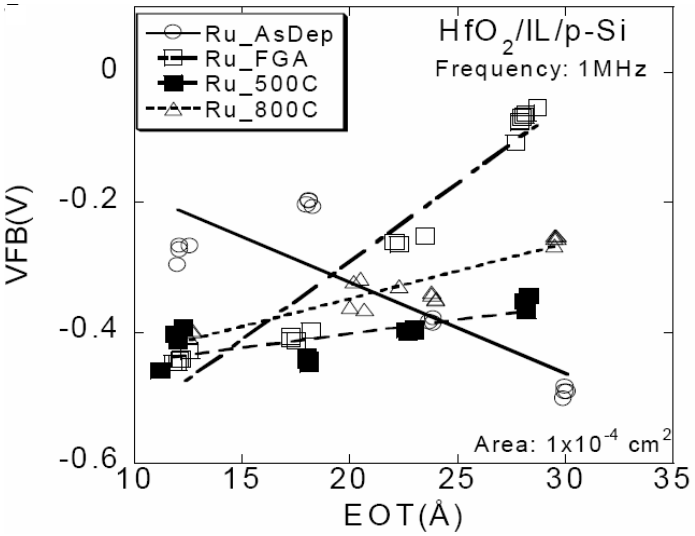


Figure 23. Flatband Voltage versus EOT for Ru/HfO_2/pSi capacitors following gate metal deposition and after various anneals

Effect of Metal Gate and Capping Layers on EOT and Effective Workfunction

Several experiments and studies have focused on the reduction of an interfacial silicon oxide by metallization located several nanometers away, on the other side of a high-k oxide film. Two of those studies, using Ti gates or AlN capping layers which have a high affinity for O, illustrate the reduction of the gate stack dielectric, in particular the interfacial layer, and even the formation of a silicide. A third, using W capping layers, illustrates the opposite, namely the ability of certain capping layers to act as a source for oxygen, which subsequently impacts the effective work function.

Thinning of Interfacial Layer and Hf-Si Formation with AlN Capping. Figure 24 shows HRTEM images of the as-deposited HfO_2/AlN stack and after annealing at 1000ºC (sample supplied by H. Alshareef/SEMATECH). After the 1000ºC RTA the interfacial SiO_2 thickness was significantly reduced. Reaction was observed at the Si/HfO_2 interface at several locations after the 1000ºC RTA (Fig. 25). AlN has a high solubility for oxygen. The thinning of the interfacial SiO_2 and the silicide reaction indicated that AlN caused the HfO_2 to become oxygen deficient by dissolution of O in the AlN. While HfO_2 in direct contact with Si should be thermodynamically stable, silicide reactions at HfO_2/Si interfaces are known to be driven by O-deficiency in the high-*k* (46). As HfO_2 is thermodynamically more stable than SiO_2, oxygen deficiency will be initially

compensated by reduction of the interfacial SiO_2, consistent with the observed thinning, until all the SiO_2 is consumed.

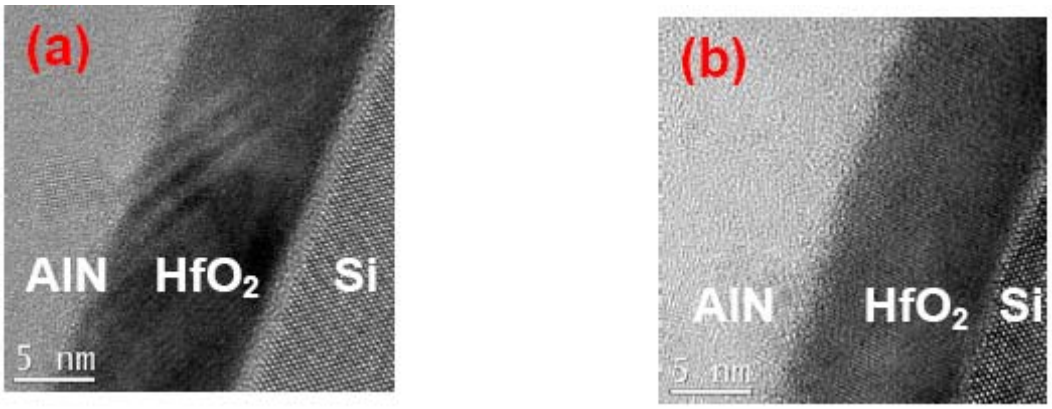


Figure 24. HRTEM images of the Si/SlN/HfO_2/Si gate stack: (a) as–deposited and (b) after 1000°C RTA. Note the thickness reduction of the SiO_2-like layer at the interface in (b).

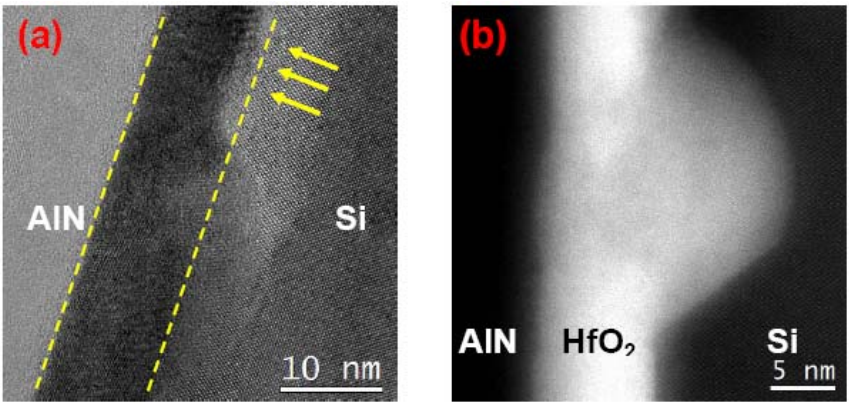


Figure 25. Interface reaction observed in the Si/AlN/HfO_2/Si gate stack after the 1000°C RTA: a) HRTEM image showing HfO_2 thinning (arrows) near the reaction phase at the Si interface, and b) HAADF image showing Hf-rich silicide reaction phase protruding into the Si substrate

Thinning of the Interfacial Layer with Ti Electrodes. To better understand the thinning of the interfacial layer with Ti electrodes, first reported by McIntyre (47), MEIS analysis was used to monitor the effect of Ti electrodes on amorphous HfO_2 films with a small amount of interfacial SiO_2 (~0.6-0.7 nm) and an excess of oxygen in the Hf oxide layer (~$HfO_{2.07}$). Backscattering spectra for this HfO_2/SiO_2/Si (001) stack were taken after Ti deposition and after a subsequent anneal to 300°C in UHV, see Fig. 26. Simulations for the HfO_2/SiO_2/Si stack after Ti deposition indicate that Ti forms a uniform layer. The oxygen concentration in the Ti layer is small immediately upon deposition (TiO_x, $x<0.10$). The Ti layer is oxidized at the outer surface (0.2-0.3 nm of TiO_x) and at the Ti/HfO_2 interface (TiO_x, $x<1$). There is a detectable amount of SiO_2 remaining at the HfO_2/Si(001) interface, however a partial depletion of oxygen from the HfO_2 layer is evident: $HfO_2+Ti \rightarrow HfO_{2-x}+V_{O\ (in\ HfO2)} + TiO_x$. After a UHV anneal of the Ti/HfO_2/SiO_2/Si (001) stack we observe a lowering and broadening of the Ti peak with growth of the oxygen yield in the region where the Ti atoms reside, indicative of oxygen incorporation in the Ti layer (up to $TiO_{0.5}$ – this is the bulk solubility of oxygen in Ti;

note that under our conditions we do not form TiO_2). There is more significant oxidation of the Ti layer at the Ti/HfO_2 interface, which can potentially change the stack capacitance compared to an ideal $TiO_\delta/HfO_2/Si$ structure, as well as the defect concentration. At the same time the decrease of the Si peak and decrease of the width of the oxygen peak are consistent with partial removal of the SiO_2 layer. Some of the Si initially present in the interfacial SiO_2 layer is most likely incorporated in the high-κ layer, as shown by more accurate modeling of the experimental data.

Rather different results were found for Ti deposition on a crystallized $HfO_2/SiO_2/Si(001)$ stack, compared to amorphous HfO_2 of the same thickness and under the same annealing conditions. After Ti deposition and UHV anneal, the amount of oxygen in TiO_x (x~0.4) film is less. More significantly, the high-energy edge of the Si peak shifts towards the Si surface peak position, indicating either some Si diffusion into the TiO_x layer or islanding of the TiO_x film on the surface. After a 600°C anneal, the surface Si peak appears, suggesting that the film is no longer continuous. This lateral non-homogeneity indicates a possible Ti-Si-O phase formation (or multiple phases): Ti + SiO → $TiSi_x$ + 3TiO. This change in the surface morphology is clear from AFM topography images, indicating that while the surface of an initially crystallized $HfO_2/SiO_2/Si(001)$ stack is basically flat, after Ti deposition and UHV annealing significant roughness (RMS = 1nm) appears (not shown). These MEIS results provide yet another example of the dramatic effect of diffusion of high-k cations, metal gate atoms, and Si atoms in these ultra-thin systems, particularly when nanocrystalline, since they can diffuse through the high k and interface layers.

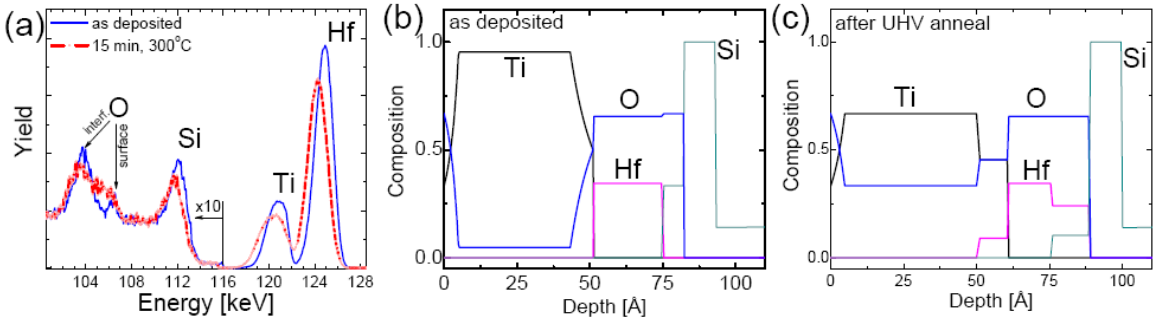


Figure 26. (a)Medium energy ion spectra for $HfO_2/SiO_2/Si(001)$ stack after Ti deposition and after Ti deposition and 300°C anneal in UHV. Incident proton energy of 130.3 keV was used with the incident direction normal to the surface and detector aligned at 125.3° . (b) and (c) Best fit elemental depth profiles for Ti, Hf, Si and O used to calculate spectra in (a)

Workfunction and EOT Stability with W Capping of MoTa Gates. Figure 27 shows the flatband voltage versus EOT for MoTa gates on SiO_2 and contrasts the results for samples having Ru capping of the metal gate with those having W capping. With Ru capping, the flatband voltages are stable up to 900°C as are the EOT's, as seen by the very slight increase in EOT going from 400°C to 900°C. With W capping, on the other hand, the effective workfunction changes by 0.5 V and the EOT increases by a nanometer. Shifts in the workfunction were quantitatively confirmed by measurements of the Fowler-Nordheim tunneling barrier height. Elemental depth profiles were measured by both RBS and AES. The RBS results, illustrated in Fig. 28 shows how the oxygen from the W capping layer piles up at the gate/dielectric interface to form both a silicate layer that

increases the EOT and an oxide at the metal in contact with the dielectric to change the effective workfunction.

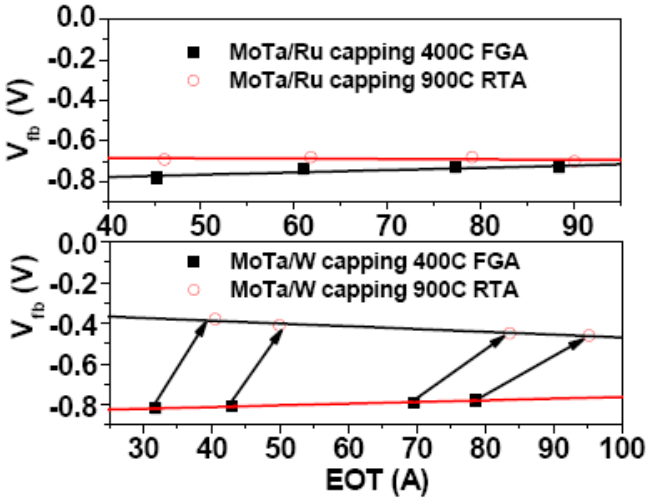


Figure 27. V_{FB} vs. EOT curves of (top) MoTa/Ru and (bottom) MoTa/W after 400°C FGA and 900°C RTA. The MoTa/Ru stack has stable work function values up to 900°C while the work function and EOT of MoTa/W increase after 900°C RTA.

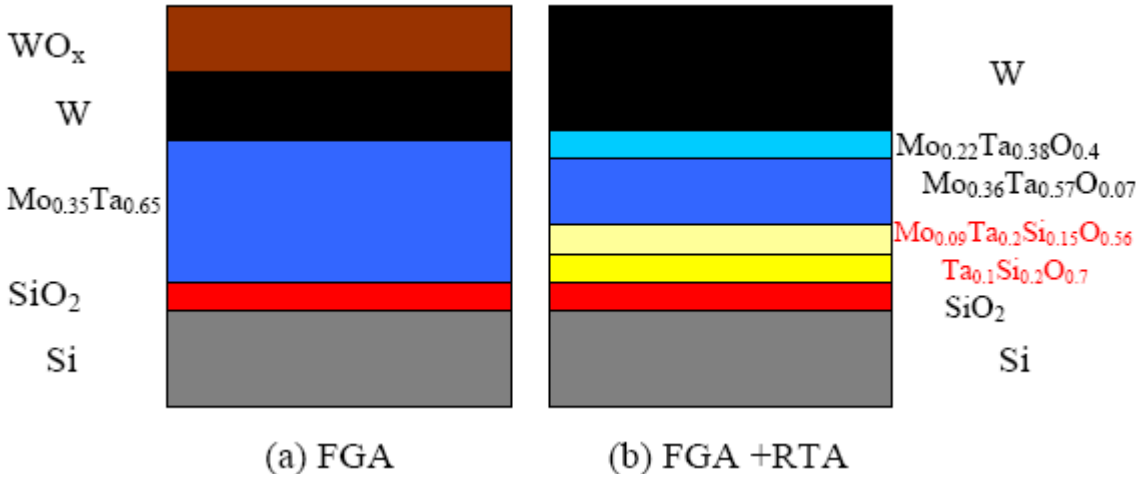


Figure 28. RBS depth profiling of (a) MoTa/W after 400°C FGA, (b) MoTa/W after 900°C RTA, where two additional layers formed at the interface of MoTa and SiO_2.

Summary and Conclusions

Considerable progress has been in the last few years made towards achieving high k gate stacks. Commercialization of these materials in VLSI technology is expected in only a few years. The SRC/SEMATECH Front End Processes Center is proud to have made a number of contributions towards this progress.

The starting point in high k gate stack formation is the interfacial layer, where the amount and position of nitrogen must be carefully controlled. Nanocrystallization has been almost universally observed in all candidate high k materials, when they are examined in HRTEM or spectroscopically. The corresponding formation of charge trapping levels associated with defects in the nanocrystalline material and the control of

threshold voltages, channel mobility, and long term reliability during stressing present one of the current challenges. Control of the workfunction of the gate electrode is shown to depend on many variables, particularly the oxygen content at the metal/high k interface. The capping layer on the metal gate was shown to play an import role in the control of this oxygen; capping layers can either be a sink for oxygen, potentially even reducing the underlying dielectric, or they can be a source for oxygen—adding to the EOT and changing the gate workfunction. The hafnium oxide family of materials, along with metal alloy gates, is seen to provide the best solution for EOT's < 0.7 nm, but higher k dialectics and thinner interfacial layers are needed below 0.7 nm.

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