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REVIEW ARTICLE

Electronic surface and dielectric interface states on GaN and AlGaN

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GaN and AlGaN have shown great potential in next-generation high-power electronic devices; however, they are plagued by a high density of interface states that affect device reliability and performance, resulting in large leakage current and current collapse. In this review, the authors summarize the current understanding of the gate leakage current and current collapse mechanisms, where awareness of the surface defects is the key to controlling and improving device performance. With this in mind, they present the current research on surface states on GaN and AlGaN and interface states on GaN and AlGaN-based heterostructures. Since GaN and AlGaN are polar materials, both are characterized by a large bound polarization charge on the order of 10^{13} charges/cm^2 that requires compensation. The key is therefore to control the compensation charge such that the electronic states do not serve as electron traps or affect device performance and reliability. Band alignment modeling and measurement can help to determine the electronic state configuration. In particular, band bending can determine how the polarization bound charge is compensated; however, the band bending is extremely sensitive to the specific processing steps such as cleaning, dielectric or metal deposition, postdeposition or postmetallization treatments, which affect oxygen coverage, carbon contamination, structural defects, bonding configurations, defect states, absorbates, and Fermi pinning states. In many cases, the specific effects of these treatments on the surface and interface states are not entirely clear as the nature of the electronic states has been obscured in complexity and subtlety. Consequently, a more systematic and methodical approach may be required. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4807904]

I. INTRODUCTION

Mitigating multilateral ecological and environmental concerns will define next-generation technology. Power electronic technologies, in particular, promise to contribute significantly to this endeavor, where GaN remains one of, if not the, most promising candidates in these technologies. The potential of GaN-based power transistors is a result of its superior material properties in comparison to other materials associated with competing technologies such as Si, SiC, and GaAs as summarized in Table I. Consequently, GaN-based technologies maintain a competitive advantage. (See Table II, where the first column presents the next major milestones needed to be achieved to advance power technologies; the second column presents the enabling feature of GaN-based technologies in achieving these milestones; and the third presents the consequential technological advantages.[1]) Specifically, the high power per unit width allows for smaller devices, which enable easier manufacturing and higher impedance; this further enables easier matching to the system, which can be complicated with other materials such as GaAs. The high breakdown voltage allows GaN-based devices to operate at higher voltages, reduces the need for voltage conversion, decreases power requirements, and simplifies cooling. Furthermore, GaN is a direct-gap semiconductor critical to light-emitting diode-technologies; utilizing this overlap in technologies will help drive down development costs.

Accordingly, a wide range of superior devices has been reported in the past several years, including heterostructure field-effect transistors (HFETs), heterojunction bipolar transistors, bipolar junction transistors (BJTs), Schottky and p-i-n rectifiers, and metal-oxide-semiconductor field-effect transistors (MOSFETs). To date, power transistors are typically Si based, which are more limited in their performance. For example, the on-resistance of Si-power MOSFETs has already been surpassed by that of GaN-power MOSFETs.[2] Furthermore, Si devices degrade at temperatures above 150 °C.[3] GaN MOSFETs [and metal-insulator-semiconductor field-effect transistors (MISFETs)] can operate at much higher temperatures, provide lower leakage currents, and reduce power consumption. GaN Schottky rectifiers have the potential for higher switching speeds and larger standoff voltages than SiC or Si, and GaN p-i-n rectifiers demonstrate high switching speeds due to the absence of minority carriers. There is also evidence that simple GaN BJTs would perform well at low current densities.[4] Moreover, AlGaN/GaN heterostructures are promising, because the disparate polarization of the materials engenders a 2D electron gas (2DEG) at the interface, which effectively reduces on-resistance and thus power loss. The consequential high electron mobility makes AlGaN/GaN heterostructures ideal for high-frequency requirements associated with HFETs and high electron mobility transistors

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TABLE I. Material properties of Si, GaAs, SiC, and GaN, where μ is the mobility, ε is the relative permittivity, E_g is the band gap energy, the BFOM ratio is the Baliga figure of merit (related to the conduction loss at low frequency), and T_{max} is the maximum temperature before degradation of the material. Reprinted from Mishra *et al.*, Proc. IEEE **90**, 1022 (2002). Copyright 2002, Institute of Electrical and Electronics Engineers.

	μ (cm^2/V·s)	ε (ratio)	E_g (eV)	BFOM (ratio)	T_{max} (°C)
Si	1300	11.4	1.1	1.0	300
GaAs	5000	13.1	1.4	9.6	300
SiC	260	9.7	2.9	3.1	600
GaN	1500	9.5	3.4	24.6	700

(HEMTs), which have demonstrated one order higher power density and higher efficiency than Si-based RF and microwave transistors. In other words, a wide range of power electronics will significantly benefit from the development of GaN and AlGaN. However, despite the promise of GaN-based electronics, there are still some issues that need to be addressed before this technology will replace existing Si-technologies: namely, developing methods of epitaxial growth of high-quality single GaN crystals, selective formation of n-type regions, and minimization of interface states between the gate dielectric and GaN or AlGaN substrate.

In this review, we address the latter. The large concentration of defects on GaN and AlGaN surfaces as well as dielectric/GaN or AlGaN interfaces results in a large leakage current and current collapse, degrading device performance and reliability; however, the mechanisms responsible for these reliability issues have not yet been fully established given the complexity of interface states. More explicitly, GaN and AlGaN are polar materials, with a large bound polarization charge at the interface that requires compensation. If the polarization charge is compensated internally, it leads to unrealistically large band bending in n-type, Ga-face GaN or AlGaN and thus, in conjunction with experimental results, suggests heavy external compensation with a large distribution of electronic surface states. Yet, the nature of these states has remained ambiguous. In the following pages, we will, therefore, summarize the current understanding of the role of electronic states in GaN and AlGaN-based devices. We look at energy band diagrams; this includes polarization charge compensation and band bending at the surface as well as band alignment modeling at the interface. Theoretical band alignment modeling includes those given by the metal-induced gap states model, the unified defect model, the disorder-induced gap states model, and the chemical reaction model. These generate band-offset values, which we will analyze in comparison to experimental measurements, highlighting the effectiveness and shortcomings of the models. In particular, we find that such models do not consistently provide reliable results. It is likely that a more comprehensive and intricate understanding of the electronic state configuration is needed to improve these models. Generally, these calculations assume a perfectly ordered interface, which is not physically achievable. This discrepancy is likely related to variations in crystal structure, differences in stoichiometry, unobserved band bending, or the presence of an interfacial oxide layer. These factors can be influenced by various processing such as wet chemical cleaning, ion sputtering, vacuum annealing, gaseous annealing, plasma annealing, dielectric passivation material and deposition method, as well as post-deposition and postmetallization treatments, which may affect oxygen coverage, organic and inorganic contamination, structural defects, bonding configurations, defect states, absorbates, pinning states, etc. In other words, understanding the role of electronic states at GaN and AlGaN is a difficult task, which is affected by many factors.

II. DEVICE RELIABILITY

As mentioned, the high concentration of electronic defect states in GaN-based electronics causes deleterious reliability issues. The most notable are the large gate leakage current in HEMTs, HFETs, and MOSFETs (or MISFETs) as well as current collapse in HEMTs and HFETs. The failure mechanisms associated with these issues have been extensively studied, but a complete understanding has yet to be described. Most studies suggest that the issues are related to hot-electron-based mechanisms, where hot electrons are trapped in defect states, and partially stress dependent, as stressing beyond a critical voltage induces additional damage likely related to the inverse piezoelectric effect.[5,6] However, the specific states that drive these mechanisms remain unclear. Furthermore, it has been suggested that the two failure modes may not be associated with one another. In other words, there are two possible distinct failure mechanisms, which may be related to different electronic states.[7] Thus, the electronic state configuration is a complex issue, and while there has been significant effort to engineer these issues out of the

TABLE II. Competitive advantages of GaN-based devices. Reprinted from Mishra *et al.*, Proc. IEEE **90**, 1022 (2002). Copyright 2002, Institute of Electrical and Electronics Engineers.

Need	Enabling feature	Performance advantage
High power/unit width	Wide band gap, high field	Compact, ease of matching
High voltage operation	High breakdown field	Eliminate/reduce step down
High linearity	HEMT technology	Optimum band allocation
High frequency	High electron velocity	Bandwidth μ-wave/mm-wave
High efficiency	High operating voltage	Power saving, reduced cooling
Low noise	High gain, high velocity	High dynamic range receivers
High temperature operation	Wide band gap	Rugged, reliable, reduced cooling needs
Thermal management	SiC substrate	High power devices with reduced cooling needs
Technology leverage	Direct band gap, enabler for lighting	Driving force for technology low cost

devices using epitaxial layer design, chip metallization, passivation schemes, and general device topology and layout,[8] it is unlikely that the devices will be fully optimized without a better understanding of their role.

A. Gate leakage

Gate leakage refers to current lost through the gate by electron tunneling, degrading power efficiency, and noise performance. In general, there are several gate leakage mechanisms typically discussed as summarized in Fig. 1, including Schottky or thermionic emission (TE),[9–15] thermionic field emission (TFE),[10–12,15–21] trap-assisted tunneling (TAT),[10,16–18,21–24] dislocation-assisted tunneling,[17,20,25–28] defect hopping,[16–18,29,30] Fowler–Nordheim tunneling,[23] Frenkel–Poole emission (FPE),[14,20,26] and space charged limited current.[31–33] The dominant mechanism in any given device may be temperature dependent, bias dependent, and device specific.

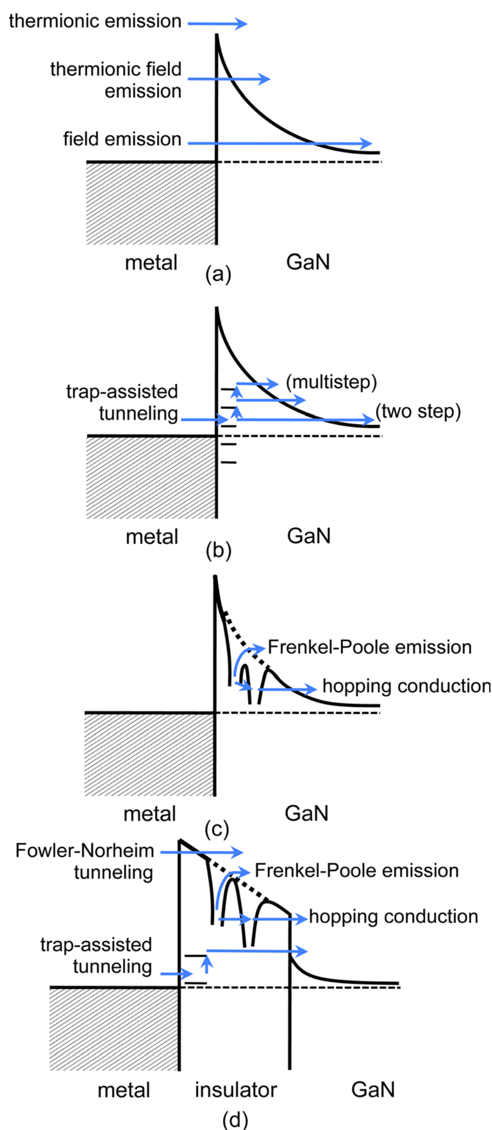

Fig. 1. (Color online) Possible gate leakage mechanisms at metal-semiconductor [(a)–(c)] and metal–insulator–semiconductor (d) interfaces.

In forward bias, the gate leakage at Schottky interfaces is often attributed to thermionic (or Schottky) emission and thermionic field emission;[9–21] however, most researchers agree that this mechanism must be coupled with another defect-related mechanism. For example, Carrano *et al.*[10] suggested that TE and TFE theories aptly describe experimental gate-leakage data only in addition to proposed deep-level bulk states that act as trapping states within tunneling distance of the interface. These defect states have been described as a continuum possibly related to the contamination layer on clean GaN, threading dislocations that reach the surface, and defects created by the Ti adhesion layer. Yu *et al.*[13] investigated the application of TE and TFE models assuming a triangular Schottky potential and also suggest that there is an enhanced tunneling component, which is demonstrated by the discrepancy of the Schottky barrier heights as measured by I-V-T and C-V measurements; the researchers, therefore, conclude that there are defects near the surface region. Shen *et al.*[31] used space charge limited current investigations to determine that deep traps $\sim$0.2 eV below the conduction band minimum are likely trapping centers. In other words, most research agrees that TE and TFE account for only a fraction of the gate leakage in forward bias; while the small theoretical emission current may be related to an uncertain evaluation of the Schottky barrier, it is clear that the gate leakage mechanism must be augmented by some trap-induced mechanism.

Reverse-bias Schottky interfaces are more influential to the gate leakage phenomenon and thus have been more extensively studied. Miller *et al.*[16,17] adapted an analytical model from the forward bias case, assuming that the current is small in reverse bias such that electrons may tunnel from the gate into the semiconductor as well as from the semiconductor into the gate. Comparisons between extensive empirical gate leakage measurements in HFETs and two-dimensional simulations suggest that vertical tunneling (or TE/TFE) is the dominant mechanism, though lateral tunneling from the edge of the gate to the drain (hopping) or TAT also contributed to the total leakage current. The leakage current is thus assumed to consist of two mechanisms that are temperature dependent. Temperature dependent modeling by Karmalkar *et al.*[18] on the off-state gate current in AlGaN/GaN HEMTs shows that TAT dominates at temperatures $<$500 K and direct TFE dominates at temperatures $>$500 K. Similarly, Zhang *et al.*[20] conducted temperature-dependent studies, suggesting the dominant mechanism at temperatures $>$150 K is FPE and at temperatures $<$150 K is TAT. Based on inferred Schottky barrier heights and room-temperature gate leakage results, they further conclude that highly conductive dislocations are likely responsible for TAT. These results are consistent with those of Kaun *et al.*,[34] who showed that decreasing the threading dislocation density from $\sim 2 \times 10^{10}$ to $\sim 5 \times 10^{7}$ cm^{-2} yielded up to a 45-fold decrease in the average reverse Schottky diode current.

The polarization may also have an integral role in the reverse-bias gate leakage mechanism. The polarization, therefore, becomes an important factor in determining device behavior as pointed out by Ganguly *et al.*[35] in InAlN/AlN/GaN devices. Similar work as been applied to AlGaN/GaN HEMTs by Yan *et al.*[26] Using the near-surface electric field

beneath the Schottky barrier, they interpret the experimental results in terms of FPE between ~300 and 450 K, concurrent with a forward TAT current. Studies by Sudharsanan *et al.*[24] show that increases in the polarization and internal electric field at the Schottky barrier occur with a simultaneous increase of gate leakage. This suggests that the leakage current mechanism must be related to defect states that also increase with the polarization. Given the lattice mismatch between AlGaN and GaN, one possibility is that an increase in aluminum concentration results in strain-induced defects, such as dislocation loops and threading segments at the interface and in AlGaN, or perhaps the increased internal electric field has induced additional defects near the surface and in AlGaN. Other studies have highlighted the importance of the electric field profile in devices, where stress-tested devices are characterized by higher leakage currents and defect densities via the inverse piezoelectric effect.[5,6] It has been argued that stress-induced defects are related to pits and grain boundaries near the gate edge where the electric field would be highest.[31,33,36–41] However, as Johnson *et al.*[42] pointed out, other defects may also be associated with the increase in postelectrical stressed devices, where the gate edge defects provide only a partial explanation for device failure. Other mechanisms such as drain-edge pits, metal diffusion, or oxide-related states as well as other native defects also influence device performance. On the other hand, externally stressing devices likely result in different behavior than increasing the polarization. It is, therefore, worth considering that an increase in polarization causes an increase in the bound charge and consequentially an increase in the compensation charge or surface states.

Such an argument would be more consistent with an alternative model proposed by Hasegawa *et al.*,[43] where the electronic states act as pinning states rather than tunnel-assisting traps. In this research, the disorder induced gap state (DIGS) model—which will be discussed later—and additional empirical results are assumed to explain the mechanism of gate leakage in AlGaN/GaN as summarized in Fig. 2(a). This work suggests that the near-surface electronic states are aptly described by a U-shaped continuum common to III-V semiconductors[44] with an additional discrete peak at E_c-0.37 eV [see Fig. 2(b)]. This discrete peak likely corresponds to a N-vacancy and thus depends on the individual sample processing treatments. In other words, the continuum is

$$N_{SS}(E) = N_{SSO} \exp\left(\frac{|E - E_{CNL}|}{E_{CNL}}\right)^{n_j}, \quad (1)$$

where N_{SSO} is the minimum surface state density, and E_{CNL} is the energy position of the charge neutrality level with respect to the valence band maximum. E_{Oj} and n_j determine the distribution shape of the continuum; j = a for acceptor-like states above E_{CNL}, and j = d for donor-donor like states below E_{CNL}. The result is that the Fermi level is pinned near E_{CNL}, generating a thin Schottky barrier (TSB) as shown in Fig. 2(c). The TSB more easily allows for electron tunneling, generating the TFE path responsible for the large leakage current in both forward and reverse directions. Hashizume *et al.*[45] later applied this model to experimental work, showing that the simulation reproduces experimental I-V-T measurements and gives excellent fitting for I-V curves in both forward and reverse bias.

In other words, defect states play an integral role in gate leakage either through a trap-based tunneling/emission mechanism or Schottky barrier pinning. Consequently, research has sought to mitigate their effects using gate dielectrics, which generate an additional barrier for tunneling and emission processes. The most recent studies have included investigations into prevalent gate dielectrics such as SiO_2,[46–50] SiN_x,[50,51] HfO_2,[52–55] Al_2O_3,[51,53–58] and AlN.[23,59] In general, these studies demonstrate an effective means of reducing the gate leakage in comparison to direct metal Schottky contacts. For example, SiO_2 and Al_2O_3 can reduce the gate leakage by three-four orders of magnitude.[47,48,51] Other studies have focused on the comparative behavior of the dielectrics. In one such study, Miyazaki *et al.*[53] compared the effectiveness of HfO_2 to Al_2O_3 on GaN metal-oxide-semiconductor heterostructure field-effect transistors (MOSHFETs). They found that Al_2O_3/GaN has a superior quality interface relative to HfO_2/GaN as demonstrated by the lower hysteresis and interface state density. Additionally, the gate leakage current of the Al_2O_3 MOSHFET is decreased by five to eight orders of magnitude in comparison to that of the HfO_2 MOSHFET. Al_2O_3/AlGaN/GaN MOSHFETs have, also, been characterized by a higher 2DEG concentration than SiN_x-passivated devices.[51] Other investigations have examined surface oxides as potential gate dielectrics and passivation schemes,[60,61] which appear to improve gate leakage currents; however, Ťapajna *et al.*[62] pointed out that although HEMTs with native surface oxide appear to effectively reduce leakage current prior to stress, such devices often see a dramatic increase in gate leakage after stress measurements. The specifics of the gate leakage mechanism in these metal–insulator–semiconductor (MIS) structures may therefore depend on the specific material and deposition method as these factors will play a role in determining the defects in the insulator and at the insulator–semiconductor interface. Liu *et al.*[23] show that in contrast with predominant thermionic field emission models for forward-bias Schottky contacts, forward bias Al_2O_3/AlGaN/GaN HEMTs are characterized by trap-assisted tunneling and Frenkel–Poole emission at temperatures $>0\,°C$ and Fowler–Nordheim emission at temperatures $<0\,°C$. Similar studies with HfO_2 (Ref. 14) also conclude that Frenkel–Poole emission is the most dominant mechanism at high temperatures. Bi *et al.*[55] have suggested that the defect states in atomic layer deposition (ALD) HfO_2 associated with this mechanism are related to oxygen vacancies, which can be passivated with a postdeposition N_2 plasma in forward biased devices—though not reverse bias where another leakage mechanism likely dominates.

B. Current collapse

Drain current collapse is the other major limiting factor in AlGaN/GaN power electronics, which describes a significant reduction in the I-V curves when measured under large-amplitude high-frequency gate swings.[63] Subsequent measurements show that there is a reduction in drain current

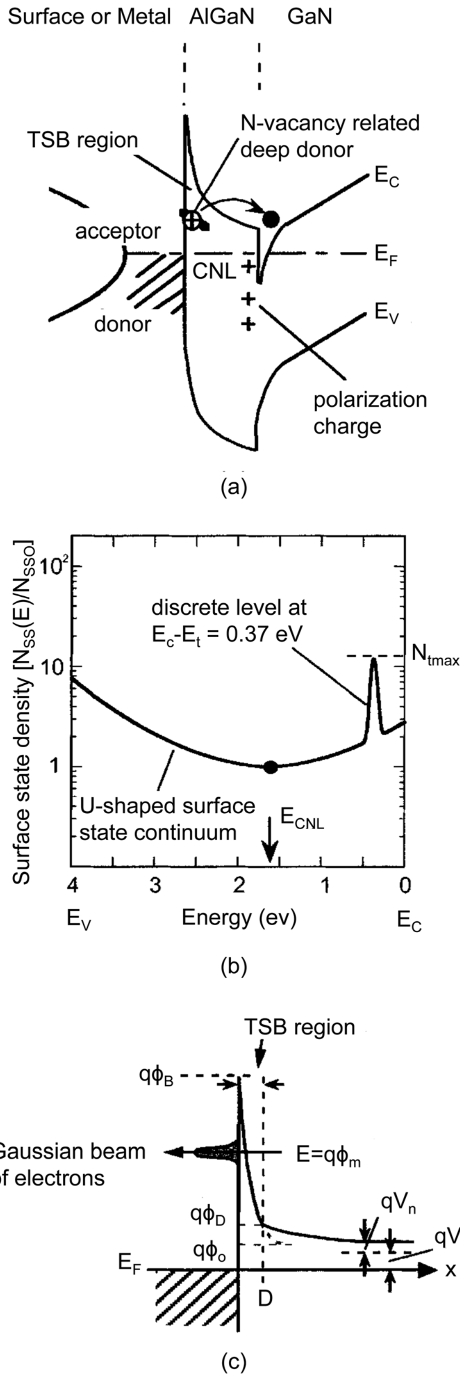

FIG. 2. (a) Unified model for near-surface electronic states of AlGaN, (b) a combined distribution of state density, and (c) the TSB model for current transport at the Schottky interface. Reprinted from Hasegawa *et al.*, J. Vac. Sci. Technol. B **21**, 1844 (2003). Copyright 2003, American Vacuum Society.

under drain stress, when the saturation region is in the on-state, and gate stress, when the channel region is pinched off in the off-state condition[64] as shown in Fig. 3(a). These results are inconsistent with other III-V MISFETs. In these devices, it is expected that on-state drain stress causes the capture of electrons from the 2DEG by deep level traps ultimately decreasing the drain current; therefore, the off-state gate stress should inject electrons back into the channel and result in an increase in drain current rather than the experimentally observed decrease.

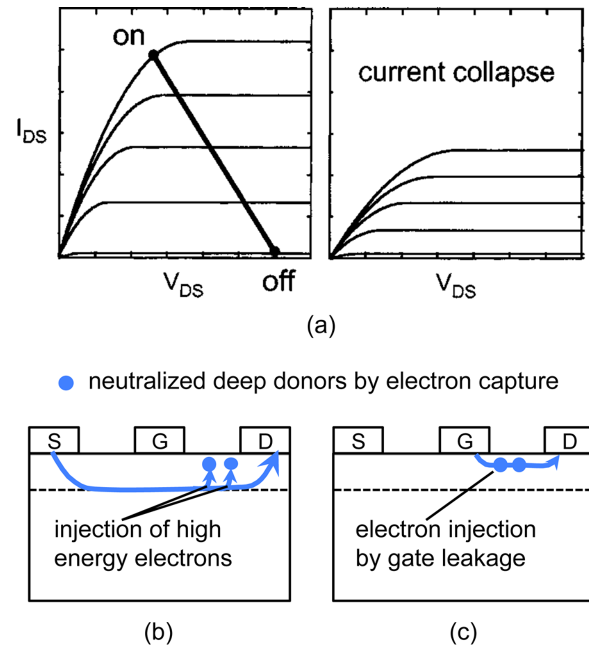

FIG. 3. (Color online) (a) Schematic representation of drain current collapse. Models presented for current collapse (b) under drain stress and (c) under gate stress. Reprinted from Hasegawa *et al.*, J. Vac. Sci. Technol. B **21**, 1844 (2003). Copyright 2003, American Vacuum Society.

Hasegawa *et al.*[43] have proposed a model to explain this behavior under drain and gate stress as summarized in Figs. 3(b) and 3(c), respectively. Using the density of states distribution in Fig. 2(a), this model assumes that electrons are injected from the 2DEG to the surface states of AlGaN near the drain under drain stress, reducing the drain current and expanding the depletion width. When the voltage is switched to the off-state, the electrons are emitted from these states leading to recovery transients, according to the following equation:

$$N_{emit}(t) = \int N_{ss}(E)\left[1 - \exp\left(-\frac{1}{\tau(E)}\right)\right] dE, \tag{2}$$

where

$$\tau(E) = \frac{1}{N_c \sigma_n \upsilon_{thin}} \exp\left(\frac{E_c - E}{kT}\right). \tag{3}$$

Hasegawa *et al.* has determined that this model fits the experimental data, where the total density of the discrete peak at 0.37 eV is 5×10^{11} defects/cm^{-2}. Once the voltage is switched back to the off-state condition, the electrons from the discrete peak are quickly emitted, giving rise to a fast transient. There is also another slower transient, which is associated with the emission of electrons from the continuum of surface states, which have a wider range of time constants and cause the formation of a virtual gate.

The concept of a "virtual gate" was proposed by Vetury *et al.*[63] in 2001. In this model, a negative surface potential behaves like a negatively biased metal gate as depicted in Fig. 4. The voltage across the gate, V_{VG}, is thus determined

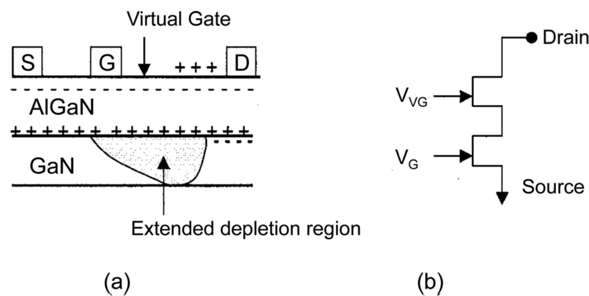

FIG. 4. Model of device showing the location of the virtual gate and schematic representation of the device including the virtual gate. Reprinted from Vetury *et al.*, IEEE Trans. Electron Devices **48**, 560 (2001). Copyright 2002, Institute of Electrical and Electronics Engineers.

by the total amount of trapped charge in the gate-drain region. In other words, this model argues that the surface of an as-grown wafer has a net positive surface charge, which arises from screening of a negative polarization bound charge. The formation of a virtual gate, therefore, arises from a reduction in this net positive charge either by removal of the positively charged defects or the trapping of electrons in donor-like defects. As trapping occurs and the states fill, the formation of the virtual gate causes an increase in the depletion region and consequent decrease in the electric field at the gate edge. The current collapse is thus related to how quickly the surface state charge is neutralized, where the trapping is strongly dependent on the electric field between the gate and the drain. To restore the current, the net positive surface charge must be replaced. This can occur with the removal of electrons from the trapping states with forward bias or the accumulation of holes at the surface. This model has since been further developed by Koudymov *et al.*[65] and Morardi *et al.*,[66] where the modeling strategy is based on a reasonable set of assumptions and a smaller number of fitting parameters. Subsequent simulations closely agree with experimental measurements in AlGaN/GaN HFETs.

Currently, the formation of a virtual gate is widely accepted as the cause of the current collapse phenomenon[67,68] and has been confirmed by several microscopy measurements;[69,70] however, it remains unclear which electronic states play a role in the creation of the virtual gate. Experimental results vary greatly—even with regards to the location of the defects in AlGaN/GaN heterostructures, which have been measured at the surface close to the gate edge,[71,72] in the AlGaN layer[71,73] at the AlGaN/GaN interface,[72,74] and in the GaN buffer.[71] Additional research has focused exclusively on traps in the GaN buffer layer in AlGaN/GaN HFETs, measuring nonlocalized trapping defects at 0.6–1.6 eV (Ref. 41) with respect to the GaN valence band maximum and in AlGaN/GaN HEMTs, measuring defects at 0.5 and 2.8 eV (Ref. 75) and 0.45 and 0.78 eV.[76] There are several likely reasons for these discrepancies. As mentioned, Marcon *et al.*[7] have suggested that reliability issues are not necessarily linked, which suggests that there are several different traps involved. Furthermore, the discrepancies suggest that the defects may be situationally specific and depend on processing conditions or device design. For example, Klein *et al.*[77,78] measured the photoionization energies of the traps at 1.8 and 2.85 eV in GaN FETs, which may have corresponded to grain boundaries or dislocations and carbon-related defects, respectively. These results are consistent with the work of Bardwell *et al.*[64] and Uren *et al.*,[79] which showed that current collapse is proportional to carbon contamination and thus dependent on the cleaning process used during device fabrication. Similarly, the presence of grain boundaries or dislocations may depend on the deposition conditions. Fehlberg *et al.*[80] suggested that the passivant deposition conditions may be more influential than the specific dielectric material after investigating the complex relationship between the stress in the SiN_x layer, the molar fraction of aluminum in AlGaN, and the transport properties of the 2DEG in HFETs. While this particular study does not specifically focus on the current collapse phenomenon, the effects of these conditions on the 2DEG concentration suggest that the strain and molar fraction may influence the condition of the trapping states. Additionally, device design also plays a role in the concentration and distribution of defects. Douglas *et al.*[81] demonstrated that there is a linear relationship between the critical degradation voltage and the gate length, suggesting that the electric field is the main cause of degradation. Similarly, Liu *et al.*[82] have shown that trap densities are dependent on the drain bias voltage. While it is possible that these defects are related to structural defects such as grain boundaries and pits, it is worth considering other alternatives as well such as oxidation or gate diffusion, which may be affected by the strong electric field. The gate material should also be considered. Esposto *et al.*[83] presented results that the diffusion may introduce traps as shown with copper gates. In other words, there seems to be very little consensus as to which defects play a role in current collapse.

Passivation schemes and gate dielectrics have also been applied to mitigate current collapse. SiN_x remains the most extensively studied dielectric, utilized in passivated HFETs (Ref. 84) and HEMTs (Refs. 85 and 86) as well as MOS-HEMTs.[87] Comparative studies between HfO_2, Al_2O_3, and SiN_x MOSHEMTs (Ref. 87) show that SiN_x is the most effective gate dielectric at reducing current collapse. However, it remains unclear whether SiN_x eliminates the trapping states responsible for the virtual gate or presents a barrier, either preventing electron trapping within these states and formation of additional negative surface charge.[88,89] In light of the current collapse mechanism presented by Hasegawa *et al.*, it would seem likely that SiN_x passivates the N-vacancy and thus reduces current collapse. This is further supported by the work of Hashizume *et al.*,[68,90,91] which finds that Al_2O_3 on N_2 plasma pretreated AlGaN is an effective passivation method in HEMTs. In this case, the passivation of the N-vacancy could be satisfied by the N_2 plasma. On the other hand, these models do not explain the surface states with slower transients, which contribute to the formation of the virtual gate. Therefore, it seems unlikely that passivation of the N-vacancy alone is enough to reduce the current collapse phenomenon. Alternatively, Kim *et al.*[92] and Gao *et al.*[67,93] have suggested that the formation of the virtual gate is a result of charging from ionized water molecules on the

device surface in a process Gao *et al*. dubbed as "electric-field-driven" oxidation. This process would be prevented by a hydrophobic passivation layer like SiN_x.

These reliability issues emphasize the importance of understanding the role of defect states in GaN-based materials, focusing on the electronic states inherent in these materials and induced by device stressing. In the rest of the review, we will focus on the former. This is not to negate the importance of the stress-dependent work, which will certainly prove crucial for device development. However, understanding the role of the electronic states inherent to these materials is a complex issue even without the extra component of additional states.

III. ELECTRONIC STATE THEORY

The electronic configurations associated with III-N technologies are fundamentally different from those of traditional silicon and other zinc-blende III-V technologies. This discrepancy is a direct result of the large polarization in III-N materials, resulting bound polarization charge, and compensating electron states. These charge states generate built-in electric fields, which play a crucial role in the electric and optical properties of these materials. In other words, there is an inherent distribution of charge in these materials, which cannot be eliminated. The goal is then to engineer the electronic state configuration to alleviate the failure mechanisms. Therefore, awareness of how electronic states may influence these properties is essential to understanding basic device behavior and future device development. The basics are thus described in the following section.

A. Surface state configurations

1. Polarization

As mentioned, GaN and other III-V nitrides are characterized by a macroscopic polarization, **P**, where **P** is the sum of the spontaneous polarization inherent to the equilibrium lattice, $\mathbf{P_{SP}}$, and the piezoelectric polarization induced by strain, $\mathbf{P_{PE}}$, as illustrated in Fig. 5.[94] Since the polarization is inherent to the material, each component can be determined from *ab initio* calculations using material constants; i.e., the elastic constants (C_{13} and C_{33}), the piezoelectric coefficients (e_{13} and e_{33}), and the lattice constants (a_o and a). Considering the strain component of the polarization along the c-axis,

$$\mathbf{P_{PE}} = 2\frac{a - a_o}{a_o}\left(e_{31} - \frac{c_{13}}{c_{33}}e_{33}\right)\hat{c}. \quad (4)$$

It is found that the piezoelectric polarization is negligible for relaxed GaN and AlN (Ref. 95) using the constant values summarized in Table III.[96–104] The spontaneous polarization, on the other hand, is large for GaN and AlN and has been calculated using the Berry-phase approach and local density[105–107] or generalized gradient approximations.[106,108] These calculations show the spontaneous polarization is negative for the Ga- and Al-face (0001) wurtzite GaN ($-0.029\,C/m^2$) and AlN ($-0.081\,C/m^2$), and thus implies that the spontaneous polarization points toward the

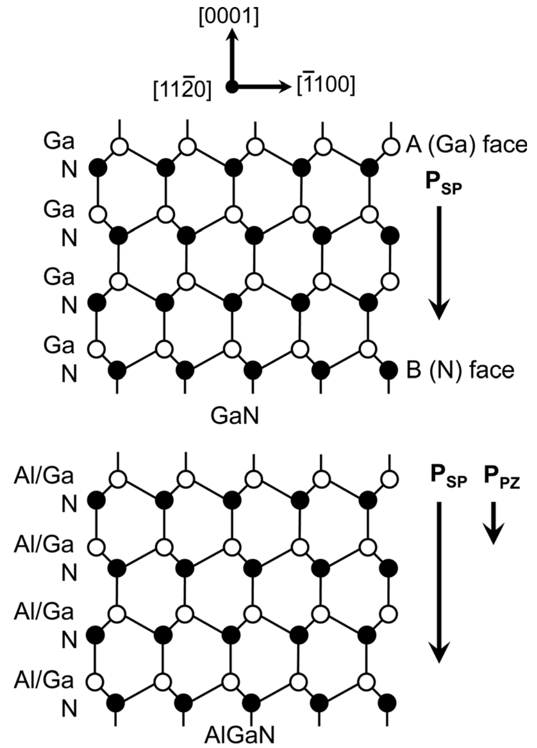

FIG. 5. Crystal structure, spontaneous polarization fields ($\mathbf{P_{SP}}$), and piezoelectric polarization fields ($\mathbf{P_{PE}}$) for GaN (top) and $Al_xGa_{(a-x)}N$ (bottom). Reprinted from Yu *et al*., J. Vac. Sci. Technol. B **17**, 1742 (1999). Copyright 1999, American Vacuum Society.

bulk. This produces a negative bound polarization charge of $\sim 1.81 \times 10^{13}$ and $\sim 5.06 \times 10^{13}$ charges/cm^2 for GaN and AlN crystals, respectively. Similarly, there will be an equivalent positive bound polarization charge on the N-face of GaN and AlN. (Note the concentration of the polarization bound charge increases with aluminum content. This is because the magnitude of the spontaneous polarization is sensitive to structural parameters, where the increase in the anion–cation bond length along the (0001) axis from GaN to AlN corresponds to an increase in the spontaneous polarization along the c-axis of the wurtzite structure.[94])

TABLE III. Lattice constants [(a) and (c)], piezoelectric constants (e_{31} and e_{33}), elastic constants (C_{13} and C_{cc}), spontaneous polarization (P_{SP}), and polarization bound charge (ρ) of GaN and AlN. The lattice and piezoelectric constants (e_{31} and e_{33}) as well as the spontaneous polarization are determined by the generalized gradient calculation as described in Ref. 106. The elastic constants are determined by an average of the values presented in Refs. 96–104. Values for $Al_xGa_{(1-x)}N$ may be determined by linear interpolation.

	GaN	AlN
a (Å)	3.189	3.112
c (Å)	5.185	3.982
e_{31} (C/m^2)	−0.37	−0.62
e_{33} (C/m^2)	0.67	1.50
C_{13} (GPa)	94.1	111
C_{33} (GPa)	348	356
P_{SP} (C/m^2)	−0.034	−0.090
ρ (cm^{-2})	2.12×10^{13}	5.62×10^{13}

Experimentally determining the spontaneous polarization has traditionally proven difficult in III-V nitrides; however, there has been some success more recently. Yan *et al.*[109] measured the thermodynamic coefficients of expansion to determine a spontaneous polarization of $-0.0219 \pm 0.0005\,\mathrm{C/m^2}$ ($\sim 1.37 \times 10^{13}$ charges/cm^2). Alternatively, Lähnemann *et al.*[110] used microphotoluminescence and cathodoluminescence spectroscopy to measure the energies of excitons in various stacking faults and self-consistent Poisson-Schrödinger equations to determine a spontaneous polarization of $-0.0220 \pm 0.0007\,\mathrm{C/m^2}$ ($\sim 1.37 \times 10^{13}$ charges/cm^2). These values are $\sim 0.01\,\mathrm{C/m^2}$ less than the theoretical values. There have been no such experimental measurements of the spontaneous polarization in AlN.

2. Band bending and tilting

Charge neutrality and Gauss's Law lead to a system where the overall charge of the system must be neutral; therefore, the large bound polarization charge of these materials must be compensated. The nature and distribution of the compensation affects the internal electric field of the materials and ultimately device performance. It is, therefore, important to understand the implications of the compensation charge distribution, which is presented in this section in terms of energy band diagram features such as band bending and bend tilting.

Band bending is an important device characteristic to consider, because it describes the energy profile of electrons at the interface: downward band bending favors the accumulation of electrons and upward band bending results in the depletion of electrons. Determination of the band bending is thus closely related to the distribution of electronic states at the interface. Consider, for example, Ga-face, n-type GaN with a doping density of $10^{17}\,\mathrm{cm^{-3}}$, and assume the negative bound polarization charge of $\sim 2.1 \times 10^{13}$ charges/cm^2 is entirely compensated internally by positive ionized donors. This type of compensation is characterized by the formation of a space-charge layer near the surface and determines surface band bending

$$\Phi_s = -\frac{qN_{SS}^2}{2\varepsilon\varepsilon_o N_d}, \qquad (5)$$

where q is the charge of an electron, ε is the relative permittivity of GaN, ε_o is the permittivity of free space, N_d is the doping density, and N_{ss} is the net charge of the surface sates in C/cm^2. This calculation would give a surface potential of -420 V, which corresponds to 420 eV upwards band bending at the GaN surface and an average electric field of 200 MV/m. In equilibrium, the large field leads to inversion or accumulation, which would limit the band bending to approximately the band gap of the material, 3.4 eV (Refs. 111 and 112) [see Fig. 6(a)]. The polarization bound charge cannot, therefore, be completely compensated internally by positive ionized donors. Experimental band bending measurements for Ga-face GaN are typically reported to be between 0.3 and 1.5 eV,[113–115] well below the band gap value. In order to achieve the experimental band bending, the depletion

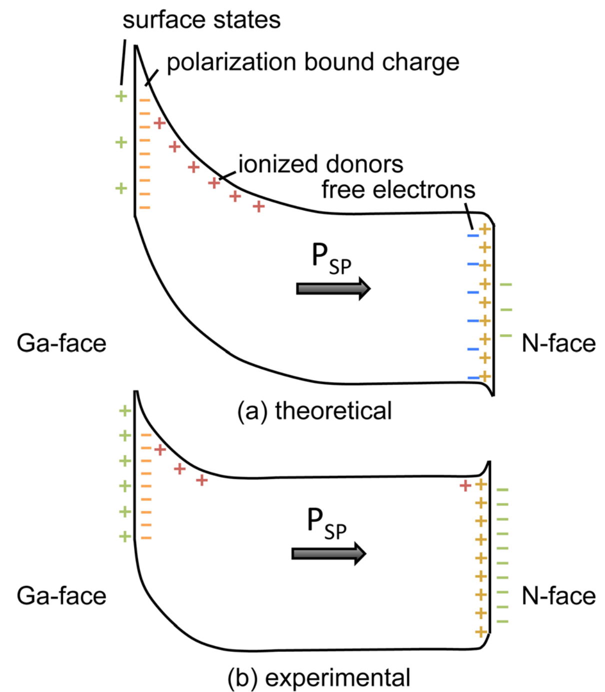

FIG. 6. (Color online) Band bending schematic for Ga- and N-face GaN. Both surfaces are screened by $\sim 10^{13}$ charges/cm^2. (NOTE: the position of the ionized donors and electrons in the material corresponds to their physical position rather than their energy level within the band gap.)

region is reduced to $\sim$56–126 nm for the doping density mentioned, which corresponds to $\sim 5.6 \times 10^{11}$–1.3×10^{12} ionized donors/cm^{-2}. Since the polarization charge will be fully compensated, the surface must be compensated by an additional $\sim 2.0 \times 10^{13}$ charges/cm^2. This compensation must therefore take place externally by charged electronic surface states [see Fig. 6(b)]. A similar argument can be made for N-face, n-type GaN with the same doping density, where assuming the bound polarization charge is maximally screened by electron accumulation results in downward band bending of 0.1 eV.[116] However, experimental measurements show upward band bending of $\sim$0.1–1.0 eV,[112,117,118] which corresponds to 2.0×10^{13} to 2.4×10^{13} surface charges/cm^2. In other words, both faces are characterized by $\sim 10^{13}$ charges/cm^2.

In other cases, the configuration of the electronic states may lead to band tilting rather than band bending, which describes the existence of a constant electric field across a material. Band tilting models are applicable to materials with no internal charge such that all charge is localized at the interfaces or surfaces. For example, in some cases, dielectrics may be characterized by a charge distribution at the surface and dielectric/substrate interface. In other cases, this model is applicable to the AlGaN layer in AlGaN/GaN-based devices, where the polarization charge at the surface and/or interface leads to a field in the dielectric. In such cases, the electric field in the dielectric or semiconductor can be determined as if it were a parallel plate capacitor.

3. Surface and defect states

As mentioned, the concentration of electronic surface states is on the order of 10^{13} charges/cm^2, which is large

compared to other materials used in devices. However, despite their importance, the nature of these states has remained elusive and intimately depends on specific deposition and processing conditions. In this subsection, we briefly discuss possible surface states, which, for simplicity, are distinguished into two types: intrinsic and extrinsic.

Intrinsic surface states are associated with an ordered reconstruction that occurs at the termination of the crystal structure. These were first presented by Tamm[119] in 1932 and Shockley[120] in 1939 in accordance with the wavefunction solutions to the Schrödinger equation at the boundary of a periodic crystalline potential, where the electron wavefunctions decay exponentially into vacuum. The distinction between the Shockley and Tamm states is associated with the method of calculation; Shockley considered the electrons with the nearly free electron approximation and thus better describes metallic surfaces, while Tamm considered the tight-binding model as expressed by linear combinations of atomic orbitals and thus better describes semiconductor materials. In 1998, Fritsch *et al.*[121] applied a similar calculation method to GaN, using the local density approximation (LDA) and the pseudopotential model to the anion- and cation-terminated (0001) surfaces of wurtzite GaN and AlN. These calculations show that the stable surface configurations differ from the bulk, where vacancy structures are thought to be the most stable configurations as shown in Fig. 7. These results agree with additional studies by Northrup *et al.*[122] and Smith *et al.*[123] However, the structure of the surface vacancy complex may also vary with the growth conditions, where metal-rich conditions favor the

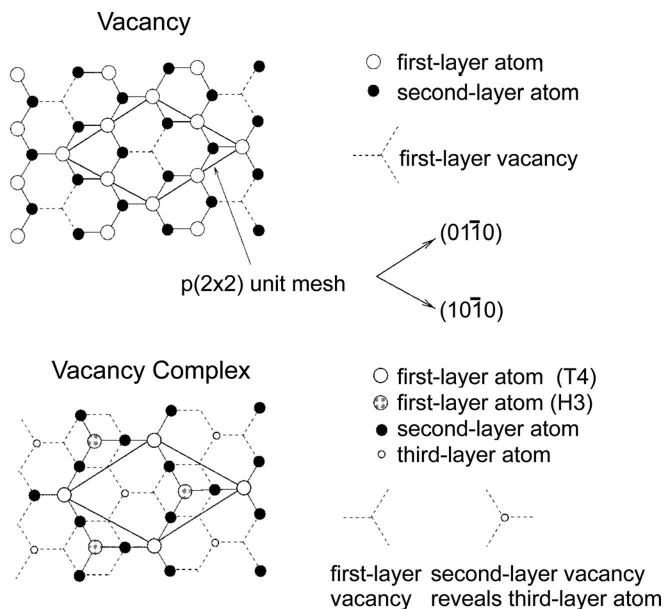

Fig. 7. Schematic top view of the vacancy and the vacancy complex. The atomic positions of the first two layers (three layer vacancy complex) are displayed. Open and closed circles represent first- and second-layer atoms. For anion termination, the white and black circles correspond to nitrogen and group-III atoms, respectively. For the case of the cation-terminated surface, the open and closed circles illustrate first-layer group-III atoms and second-layer nitrogen. The $p(2\times2)$ unit cell used in all calculations is indicated. Reprinted from Fritsch *et al.*, Phys. Rev. B **57**, 15360 (1998). Copyright 1998, American Physical Society.

adsorption of a metal adlayer on the cation-terminated surface. This reconstructed surface determines the electronic surface states on AlN and GaN, where the hexagonal reconstruction is the most likely for both materials,[121] which leads to extensive dangling bonds and vacancies.

Any deviation from this perfectly reconstructed surface is associated with extrinsic surface states. In GaN and AlN, these defects are likely to be extensive and include variations in surface reconstructions, grain boundaries, dislocation defects, structural defects, and native oxides as well as absorbates such as oxygen, carbon, and hydrogen, each with their own corresponding energy and charge states. Which states are influential depends on the deposition, cleaning, and processing methods and conditions. Experimental research shows that the band bending on GaN is upwards regardless of the crystal orientation, which indicates positively charged states on the Ga face and negatively charged states on the N face. It has been posited by French[124] that the most likely states are structural defects, Ga termination, surface contamination (such as absorbed oxygen atoms), surface states, absorbates, or additional charge compensation.

B. Interface state configurations

Interface electronic states are further complicated as the interface formation process may generate additional defect states. Over the past century, several models have been developed and refined to describe a semiconductor interface. However, the subtlety and complexity of interface electronic states have frustrated attempts to create a unified predictive theory. The original concept of interface modeling was presented independently by Schottky[125] and Mott.[126] This model can be derived for metal–semiconductor interfaces such that the Schottky barrier height (SBH, Φ_B) is described by the difference between the work function of the metal, ϕ_M, and the electron affinity of the semiconductor, X_S, as shown in Fig. 8(a),

$$\Phi_B = \phi_M - X_S. \tag{6}$$

The Schottky–Mott model assumes that the metal and semiconductor are at equilibrium, such that there is no charge transfer or direct interaction and therefore no dipole across the interface. The simplicity of this model proves ineffective at determining experimental results, which often demonstrate little dependence on the metal work function. This led Bardeen[127] to adapt the model in 1947 to include interface states. Bardeen recognized that a low density of interface states energetically located in the semiconductor gap could sufficiently "pin" the Fermi level. Therefore, as the metal and semiconductor are brought into contact, charge can flow across the interface to fill or deplete the surface states in the semiconductor. This charge transfer results in an interfacial dipole, Δ, which can then freely compensate the difference between the metal and semiconductor work functions as shown in Fig. 8(b) and summarized in the following equation:

$$\Phi_B = \phi_M - X_S - \Delta. \tag{7}$$

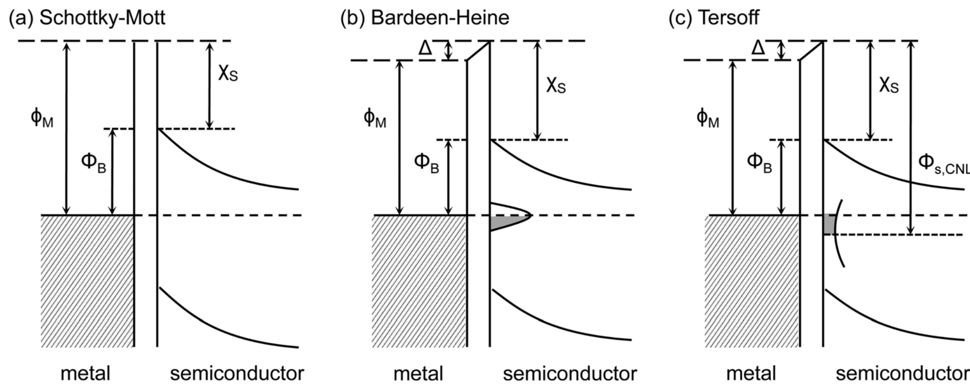

FIG. 8. Schematic of the metal–semiconductor interface models according to (a) Schottky–Mott, (b) Bardeen–Heine, and (c) Tersoff.

In 1965, Heine[128] further advanced this model by elaborating on the nature of the surface defects in the Bardeen model. The Bardeen–Heine model points out that localized states cannot exist at the interface when coupled to a continuum of free electrons present in the metal, but rather the tails of the electron wavefunctions will decay into the semiconductor and induce states within the band gap. These states have come to be known as metal-induced gap states (MIGS). In 1977, Flores and Tejedor[129] argued that the metal-like behavior responsible for the MIGS in the metal/semiconductor heterostructure is also applicable to semiconductor/semiconductor heterostructures. The interface dipole is thus induced when the charge neutrality points of the two semiconductors are not aligned at the interface.[130] Tersoff[131] further refined this concept, arguing that the single most important property at a semiconductor heterostructure is the "line up," which occurs to minimize the interface dipole as shown in Fig. 8(c). In other words, the semiconductors will align at the charge neutrality point rather than at the electron affinity. The resulting SBH gives

$$\Phi_B = S(\phi_M - \Phi_{S,CNL}) + (\Phi_{S,CNL} - X_S), \tag{8}$$

where $\Phi_{S,CNL}$ is the charge neutrality point with respect to the vacuum level, and S is the Schottky pinning factor. This factor determines the strength of the Fermi pinning; in the absence of pinning, $S = 1$, reducing Eq. (8) to the Schottky–Mott model, while in the limit of strong pinning, $S = 0$, pinning the barrier height at the charge neutrality level (CNL) of the semiconductor. However, even decades after Tersoff first proposed this theory, the scientific community has continued to explore for a unified theory, where the major point of contention is the nature of the charge transfer at the interface. Some models, as with the electron affinity model, maintain that there is no charge transfer at the interface. Others detail the nature of the charge transfer, and a subset of these models account for the nature of the transfer differently with regards to the various states responsible for Fermi pinning and the position of the charge neutrality level.

1. Schottky pinning

As mentioned, the Schottky pinning factor (S) is intricately linked to the interface defect density; however, this requires a fundamental understanding of the interface defects, which has remained elusive. Consequently, several models exist to explain this phenomenon. These include the MIGS model, the unified defect model, the DIGS model, and the chemical reaction model.

As previously mentioned, the MIGS model assumes that there are intrinsic states within the energy gap of the semiconductor, which can be related to the exponential decay of the electron wave functions from a metal when in intimate contact with a semiconductor as shown in Fig. 9(a). Mönch[132] compiled results of barrier heights at M-S interfaces with respect to their dielectric constants, giving a semi-empirical theoretical expression for the Schottky pinning factor

$$S = \frac{1}{1 + e^2 N_{MIGS}\delta/\varepsilon\varepsilon_o}, \tag{9}$$

$$= \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}, \tag{10}$$

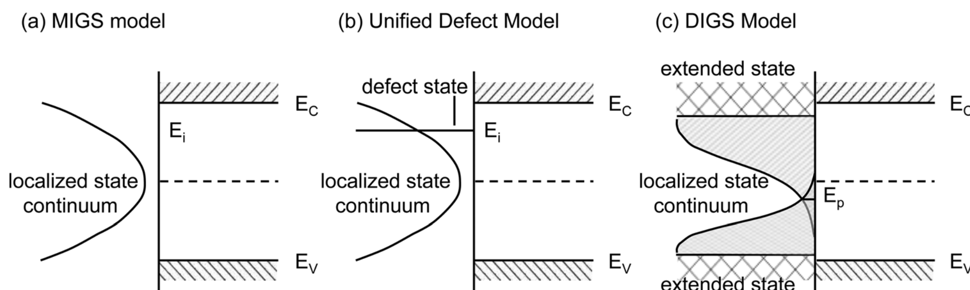

FIG. 9. Schematic representation of the interface defect densities according to (a) the MIGS model, (b) the unified defect model, and (c) the DIGS model (or the positional surface disorder model).

where N_{MIGS} is the density of interface states per unit area, δ is their extent into the semiconductor, and ε_∞ is electronic permittivity of the semiconductor. This model has also been used to describe insulator/semiconductor interfaces with some success, though it is unclear where MIGS would originate in such a system.

Spicer *et al.*[133,134] noticed that for III-V compounds the pinning phenomenon occurs not only at metal/semiconductor heterojunctions but also at oxide/bulk semiconductor interfaces. Furthermore, the Fermi level stabilizes after a fraction of a monolayer of oxide or metal is added to the surface before MIGS could be fully established. They, therefore, suggest that the pinning is a result of the interaction between the adatoms and the semiconductor surface regardless of the electronic configuration of the adatom. This results in a new model for pinning based on interface defect states, where defect formation is caused by the energy released when the atom is adsorbed. The thermal energy produced by chemisorption of an adatom can excite a constituent atom from the semiconductor, generating a vacancy as shown in Fig. 10, and the vacancy states characterize Fermi level pinning. These localized defect states coexist with the usual U-shaped continuum as shown in Fig. 9(a). However, this model can be problematic, as it requires explicit identification of defect states on an atomic level and fails to explain many experimental results. Furthermore, it has yet to be explicitly applied to GaN-based studies.

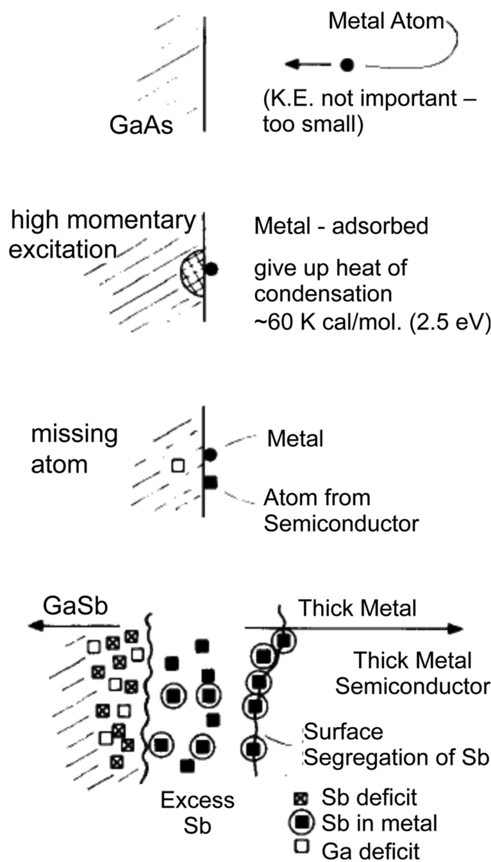

Fig. 10. Schematic of suggested defect mechanism due to deposition of metal atoms on clean III-V surfaces. This process (i.e., a defect must be formed) needs to occur only about once for every hundred metal atoms striking the surface to account for Fermi level pinning. Reprinted from Spicer *et al.*, J. Vac. Sci. Technol. **16**, 1422 (1979). Copyright 1980, American Vacuum Society.

Hasegawa *et al.*[135] have proposed a similar model where the disorder induced at the surface region of the semiconductor is responsible for pinning as shown in Fig. 9(c), where departure from the crystalline structure generates "Anderson localized states." It is assumed that these defect states are several monolayers thick and energetically distributed within the energy band gap. These assumptions were based on experimental C-V and photocapacitance transient spectroscopy measurements that showed: (1) all N_{ss} distributions are U-shaped, which are characterized by a minimum density, $N_{ss,min}$, at E(min) and the radius of curvature; (2) the magnitude of $N_{ss,min}$ and the radius of curvature are sensitive to sample species and processing. (For example, high-temperature annealing resulted in higher $N_{ss,min}$ and sharper curvature.); (3) E(min) corresponds to the CNL and fluctuates very little with processing steps, typically $<\pm 0.05$ eV; and (4) the Fermi level is pinned at this level.[44] In Fig. 11, Hasegawa explicitly summarizes how various bonding configurations affect the distribution of states. This gives rise to the following Schottky pinning factor:[136]

$$S = \mathrm{sech}(\delta/\lambda), \tag{11}$$

where

$$\lambda = \sqrt{\varepsilon\varepsilon_o / e^2 N_{DIGS}(E_o)}, \tag{12}$$

δ is the thickness of the disorder layer and $N_{DIGS}(E_o)$ is the volume density of DIGS at E_o.

On the other hand, most of the models overlook the chemical reactivity, which has been challenged by Andrews and Phillips.[137] In particular, they noticed a strong linear correlation between the heat of formation, ΔH_f, and the SBH, which is consistent with what the researchers called "moderately strong" bonding on Si. Brillson[138] conducted a similar study on compound semiconductors. The curves

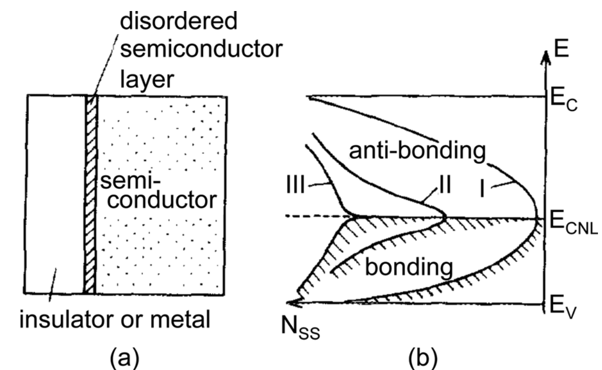

Fig. 11. Unified DIGS model explaining the correlation between I-S and M-S interfaces. Surface disorder introduces DIGS whose density depends on the degree of disorder (I: good I-S interface, II: poor I-S interface, and III M-S interface). The physical meaning of E_{CNL} can be interpreted as the Fermi energy of the DIGS spectrum where charge neutrality is achieved. E_{CNL} is the branch point between the bonding and antibonding states in the gap. Reprinted from Hasegawa and Ohno, J. Vac. Sci. Technol. B **4**, 1130 (1986). Copyright 1986, American Vacuum Society.

show a strong correlation between reactive ($\Delta H_f < 0$) and nonreactive ($\Delta H_f > 0$) interfaces. While this model does not give rise to an explicit microscopic explanation of the Fermi level pinning, it does suggest that the chemical reactivity may affect the interface states and SBH. To date, such studies have not been reported on GaN or AlGaN.

2. Band line-up

In addition to the nature of Schottky pinning, there is also debate as to the point of alignment at a heterojunction, and again, the electron affinity and the charge neutrality level models have been considered. The electron affinity is the classical point of alignment as proposed by the Schottky–Mott model, which was later adapted by Anderson[139] for semiconductor/semiconductor heterojunctions. However, this model represents an idealized case and assumes no charge transfer at the interface.

The charge neutrality level is an alternative point of alignment at a heterostructure, where the concept is central to Fermi-level pinning and charge transfer. As previously mentioned, the charge neutrality level is essentially the energy where the gap states cross from donor-like to acceptor-like. (In one dimension, this energy corresponds to the branch point energy, E_B). In other words, the CNL is the weighted average of the density of states as shown in Fig. 12. This value can be calculated from the band structure as the energy at which the simple Green's function is zero[140,141]

$$G(E) = \int_{BZ}\int_{-\infty}^{\infty} \frac{N(E')dE'}{E - E'} = 0, \tag{13}$$

where the density of states, $N(E')$ can be determined by the local density approximation[131,140,141] or the empirical tight bonding model (ETB).[143] In the LDA, the approximate electron density at each point is applied to the exchange energy in density functional theory (DFT) to determine the electronic band alignment. A consequence of this approximation is that the band gaps are typically too small and must be adjusted to the experimental values. In the ETB, the Bloch functions are derived assuming the electrons are tightly bound to the ionic cores of the constituent atoms. A simplified version of this calculation has been presented by Cardona and Christensen[142,143] to provide quicker calculations. To accomplish this, they used Baldereschi's concept of mean-value points in the Brillouin zone.[144] The power of these methods is that they find the band offsets in terms of the semiconductor bulk properties for a wide range of bonding types without the need to characterize each bond explicitly. This is particularly useful for amorphous structures, where specific bonding structures may be difficult to characterize.

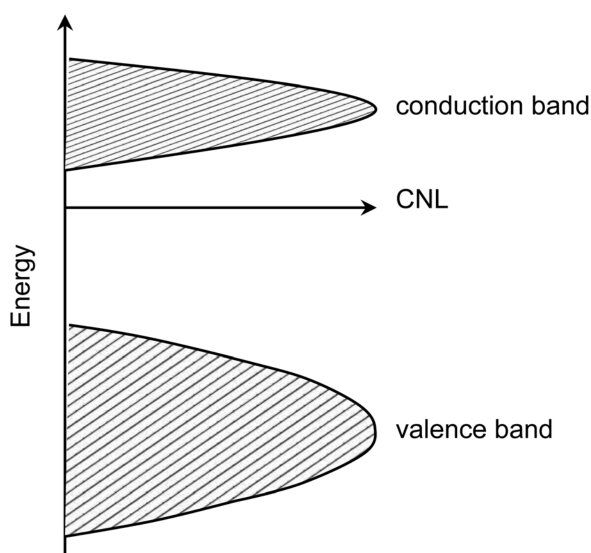

Fig. 12. CNL is a weighted average of the density of states. It is repelled by a large density of states in the valence or conduction band. Reprinted from Robertson and Falabretti, J. Appl. Phys. **100**, 014111 (2006). Copyright 2006, American Institute of Physics.

There have been other attempts to develop a model using explicit interface bonding as shown by Van de Walle,[145,146] which rely on a complete description of the interfacial electronic distribution. This is accomplished by self-consistent calculations based on local DFT, applied momentum space formalism, and nonlocal norm-conserving pseudopotentials. In these calculations, the band gaps more accurately reflect the experimental values.[147] In another model as presented by Wei and Zunger,[148] the natural band offsets are determined using a first-principles band structure method, using the LDA in DFT as implemented by the general potential, relativistic, all electron, linearized augmented plane wave method, and the Ceperly Alder exchange correlation potential. While this method does not calculate the CNL explicitly, Robertson[141] later revised the calculations to deduce the CNL for comparison. These results were later corrected to account for the changes in the valence band maximum because of hydrostatic volume deformation.[149] The calculated results from these models for GaN and AlN are summarized in Table IV.[141,143,146,148–152]

It is worth pointing out that the CNLs of III-V semiconductors have shown some interesting trends as calculated by Mönch.[143,153] In general, the CNL lies at the average bonding–antibonding gap, rather than at the minimum of the direct or indirect gap. With increasing polarity or ionicity, the valence bands becomes flatter as associated with a higher effective mass, and the conduction bands becomes increasingly direct with respect to the valence band maximum and a smaller density of states at the band edge. The CNL of higher

Table IV. Summary of band gap, electron affinity, and charge neutrality levels for GaN and AlN, where the CNL is included for several different methods of calculation including the tight binding (ETB) (Ref. 143), LDA (Ref. 141), and two different first principle (FP) calculations (Refs. 146 and 148) as well as the experimental values (Refs. 149–152), which are deduced from Schottky barrier measurements.

			CNL				
	Band gap	EA	ETB	LDA	FP_1	FP_2	Expt.
GaN	3.4	3.3	2.37	2.88	2.17	2.14	2.45–2.50
AlN	6.2	0.6	2.97	3.97	2.87	2.94	
$Al_xGa_{(1-x)}N$			$xX_{AlN} + (1-x)X_{GaN}$				

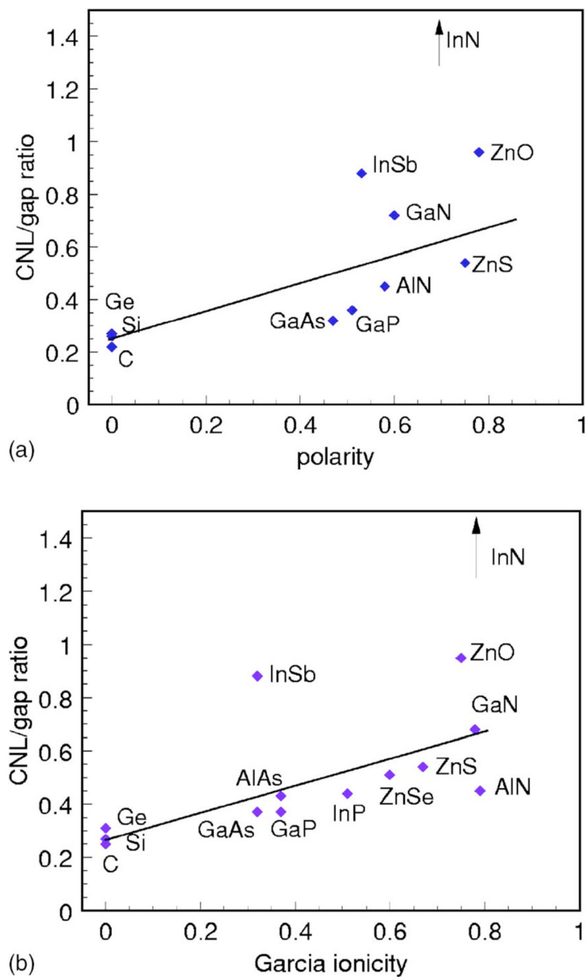

FIG. 13. (Color online) Trend of the CNL/band gap ratio vs. (a) Harrison's bond polarity and (b) ionicity of Garcia and Cohen. As the band gap becomes more direct with higher ionicity, the CNL moves higher in the gap. Reprinted from Robertson and Falabretti, J. Appl. Phys. **100**, 014111 (2006). Copyright 2006, American Institute of Physics.

polarity materials, i.e., GaN and AlN, is repelled by the higher density of states in the valence band and thus occurs higher in the band gap as shown in Fig. 13. This is noteworthy in connection with the chemical reactivity model, where an increase in reactivity or ionicity is mirrored by an increase in the Schottky barrier at a Schottky interface. For the two models to be consistent, it would imply charge transfer at the interface, which is manifested in the minimization of the interface dipole or strong Fermi pinning. The nature of the interface dipole is thus the distinguishing factor in these models. Therefore, in cases where there is little or no charge transfer, the models should be in close agreement as there is no pinning factor. Furthermore, the reduction of the interface dipole results in a similar alignment, and the charge neutrality level and electron affinity models will provide similar results.

3. Band offsets

These band alignment models ultimately describe the band offsets, which are relevant to the confinement properties of carriers in the semiconductor. To date, the most extensive theoretical studies of the band offsets for various

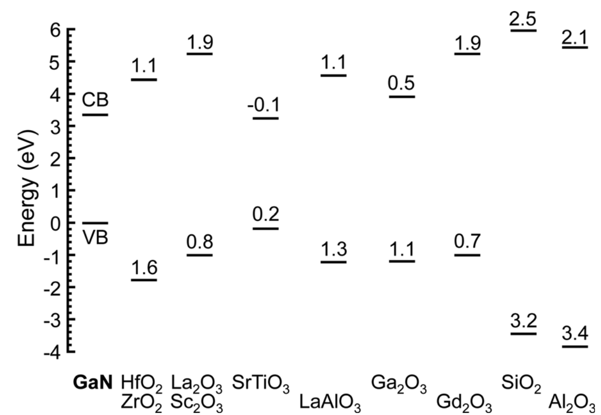

FIG. 14. Calculated band offsets of dielectrics on GaN. Reprinted from Robertson and Falabretti, J. Appl. Phys. **100**, 014111 (2006). Copyright 2006, American Institute of Physics.

dielectric/GaN interfaces have been conducted by Robertson and Falabretti,[141] using the MIGS pinning factor and CNL alignment as determined by the LDA. According to this model, the valence band offset (VBO) can be determined as

$$\Delta E_V = E_{CNL,oxide} - E_{CNL,GaN} - S[I_{GaN} - I_{oxide} - (E_{CNL,GaN} - E_{CNLoxide})], \quad (14)$$

where I is the photo threshold energies, and E_{CNL} is the charge neutrality level with respect to the valence band maximum for GaN and the respective oxide. The results as calculated by this model are summarized in Fig. 14 and Table V. Additionally, there have been a few publications on band offsets using first-principle and *ab-initio* calculations that analyze specific bonding configurations; studies by Zhang *et al.*[154] determined the conduction band offset (CBO) for

TABLE V. Valence band and conduction band offsets calculated for dielectrics on GaN as calculated by the local density approximation and charge neutrality level model (Refs. 141 and 189). All band offsets are given in eV.

	Band offset	
Material	VBO	CBO
AlN	0.4	2.4
Al_2O_3	3.0	2.4
Ga_2O_3	0.7	0.5
Gd_2O_3	0.7	1.9
$GdScO_3$	0.1	2.6
HfO_2	1.6	1.1
$HfSiO_4$	1.7	1.6
$LaAlO_3$	1.3	1.1
La_2O_3	0.7	2.0
MgO	2.0	2.6
$PbTiO_3$	−0.2	0.4
Sc_2O_3	0.7	2.0
Si_3N_4	0.8	1.3
SiO_2	3.1	2.6
$SrTiO_3$	0.2	−0.1
Ta_2O_5	1.1	0.1
Y_2O_3	0.8	1.9
ZnO	0.9	−0.7
ZrO_2	1.6	1.1

TABLE VI. Valence band and conduction band offsets measured for dielectrics on GaN. If one of the offsets is deduced from the measured band offset and the band gap, it is denoted with "a." The deposition method is noted, where ALD = atomic layer deposition, dry term. ox. = dry thermal oxidation, E-beam = electron beam, ECR = electron cyclotron resonance, MBD = molecular beam deposition, PEALD = plasma-enhanced atomic layer deposition, PECVD = plasma-enhanced chemical vapor deposition, PEMBD = plasma-enhanced molecular beam deposition, and pulsed laser = pulsed laser deposition. In addition, the characterization method is noted, where CV = capacitance-voltage measurements, EELS = electron energy loss spectroscopy, PL = photoluminescence, UPS = ultraviolet photoelectron spectroscopy, UV = UV adsorption, UV-vis = UV-visible adsorption, and XPS = x-ray photoelectron spectroscopy. All offsets are given in eV.

				Band offset		
Material	Deposition	Specifics	Characterization	VBO	CBO	Reference
AlN	ECR MBD		*In-situ* XPS	0.8	2.0[a]	168
	reactive MBD	Al + NH_3	*In-situ* XPS	1.4	1.4[a]	169
Al_2O_3	PEALD	DMAI + O_2 plasma	*In-situ* XPS and UPS	1.8	1.3[a]	111
	ALD	TMA + H_2O	*Ex-situ* XPS and UPS	0.1	3.0[a]	170
	ALD	TMA + H_2O	XPS	1.2	2.0	171
	ALD	TMA + H_2O	CV		2.1	172
CaO	MBD	H_2-less	XPS	1.0	2.5[a]	156
Ga_2O_3	dry therm. ox.		XPS	1.4	0.1[a]	173
$(Gd,Ga)_2O_3$	E-beam	$Ga_5Gd_3O_{12}$	*Ex-situ* XPS	1.1	0.9	157
$GdScO_3/SrTiO_3$	MBD		XPS	0.4	2.0[a]	163
HfO_2	PEALD	TEMAH + O_2 plasma	*In-situ* XPS and UPS	1.4	1.0[a]	111
	ALD	TEMAH + H_2O	*Ex-situ* XPS and UPS	−1.9	4.3[a]	170
	ALD	TDMAH + H_2O	XPS	0.5	1.5	171
	MBD	Hf MBD + O_2 plasma	*In-situ* XPS and UPS	0.3	2.1[a]	174
	Sputtering	Sputtering Hf + O_2	XPS, UV	0.6	1.7	175
HfAlO	ALD	TMA/TDMAH + H_2O	XPS	0.8	1.6	171
$LaAlO_3/SrTiO_3$	MBD		XPS	−0.3	2.5[a]	163
La_2O_3	MBD		XPS	1.9	0.9[a]	160
$(La_2O_3)_{0.5}(SiO_2)_{0.5}$	Pulsed Laser	Laser + La_2O_3,SiO_2	XPS, EELS	0.9	1.4	158
$Mg_{0.5}Ca_{0.5}O$	PEMBD	Ca Mg MBD + O_2 plasma	XPS, PL	0.7	3.4[a]	159
MgO	MBD	Mg MBD + O_2	XPS	1.2	3.2[a]	176
	PEMBD	Mg MBD + O_2 plasma	XPS	1.1	3.3[a]	177
Sc_2O_3	MBD		XPS	0.8	2.1[a]	160
	PEMBD	Sc MBD + O_2 plasma	XPS	0.4	2.1[a]	161
	Pulsed Laser		XPS	0.8	2.0[a]	162
Si_3N_4	MBD	Si MBD + N_2 plasma	*In-situ* XPS	−0.6	2.5[a]	178
	PEMBD		XPS	−0.4	2.4[a]	179
	ECR-PECVD	N_2 + SiH_4	XPS	1.0–1.2		180
SiO_2	ALD	APTES + O_3 + H_2O	XPS	2.4	3.0	171
	MBD	Si MBD + O_2 plasma	*In-situ* XPS and UPS	2.0	3.6[a]	181
$SrTiO_3$	MBD	SrO + (Ti + O_2)	XPS	0.1	−0.2[a]	163
ZnO	PEMBD	Zn MBD + O_2 plasma	*Ex-situ* XPS and UPS	0.8	−0.8[a]	164
	Sputtering		XPS, PL UV-vis	0.5	−0.6	165
	Sputtering		Temp-dependent IV	0.5[a]	−0.6	166
	Sputtering		XPS	0.7	−0.7	167

[a]Estimated value.

$PbTiO_3$/GaN as 0.4 eV, and research by Nakayama and Murayama[155] approximately determined the conduction band offset for ZnO/GaN as 1.6 eV. However, they also cite a large range of values from 1.0 to 2.2 eV, depending on the surface processing, which suggests that the processing steps may be crucial when analyzing the band alignment models if such processing alters the interfacial bonding. Experimental band alignments for dielectrics on GaN are summarized in Table VI.[111,156–181] Comparisons between the theoretical and empirical values—see Table VII[141,160–181]—show that the model affords a good approximation for some heterostructures such as those with Sc_2O_3,[160–162] $SrTiO_3$,[163] and ZnO.[164–167] However, the model is not as reliable for other interfaces such as those with AlN,[168,169] Al_2O_3,[111,170–172] Ga_2O_3,[173] HfO_2,[111,170,171,174,175] La_2O_3,[160] MgO,[176,177] Si_3N_4,[178–180] and SiO_2.[171,181]

These discrepancies are likely related to variations in crystal structure, differences in stoichiometry, unobserved band bending, or the presence of an interfacial oxide layer. In some cases, the discrepancy can be understood in terms of the band gap. This is the case for Al_2O_3, where the band gap ranges from 8.8 to 6.2 eV for α-crystalline to amorphous structures and is, therefore, dependent on the method of oxide film growth. The decrease in the band gap has been associated

TABLE VII. Comparison between the theoretical band offset calculations (Ref. 141) and experimental measurements (Refs. 160–181). Materials that are characterized by a discrepancy >0.4 eV are shown in bold. All band offsets are given in eV.

Material	Deposition	Band offset VBO	Band offset CBO
AlN	CNL	0.4	2.4
	ECR MBD	0.8	
	Reactive MBD	1.4	
Al_2O_3	CNL	3.0	2.4
	PEALD	1.8	
	ALD	0.1	
	ALD		2.1
	ALD	1.2	2.0
Ga_2O_3	CNL	0.7	0.5
	Dry therm. ox.	1.4	
HfO_2	CNL	1.6	1.1
	PEALD	1.4	
	MBD	0.3	
	ALD	−1.9	
	ALD	0.5	1.5
	Sputtering	0.6	1.7
La_2O_3	CNL	0.7	2.0
	MBD	1.9	
MgO	CNL	2.0	2.6
	PEMBD	1.1	
	MBD	1.2	
Sc_2O_3	CNL	0.7	2.0
	PEMBD	0.4	
	Pulsed laser	0.8	
	MBD	0.8	
Si_3N_4	CNL	0.8	1.3
	MBD	−0.6	
	PEMBD	−0.4	
	ECR-PCVD	1.0–1.2	
SiO_2	CNL	3.1	2.6
	MBD	2.0	
	ALD	2.4	3.0
$SrTiO_3$	CNL	0.2	−0.1
	MBD	0.1	
ZnO	CNL	0.9	−0.7
	MBD	0.8	
	Sputtering	0.5	−0.6
	Sputtering		−0.6
	Sputtering	0.7	−0.7

with defect-induced states located in the band gap,[182] where the valence band maximum states are associated with the O 2p states, and the conduction band minimum states are associated with the Al 3s, 3p states.[124] Rehybridization between Al 3s, 3p, and O 2p modifies the charge transfer between Al and O, and consequently decreases the band gap, increasing the valence band maximum. This explains why the results described in Table VI show similar values for the CBO but a wide range of values for the VBO—though it does not explain the VBO of 0.1 eV, which is much lower than the other presented values deposited by a similar method. MgO has also shown band gap narrowing, where the band gap difference from crystalline MgO (7.8 eV) to amorphous MgO (6.1 eV) (Ref. 183) is manifested in the valence band. This may account for the discrepancy in the MgO results as well. In other cases, such as HfO_2, there is a large range of experimentally measured offsets. It is possible that these fluctuations occur because of inconsistent processing methods, such as cleaning and deposition technique, which may result in varied oxygen coverage, dielectric stoichiometry, and interfacial bonding. Since the bonding configuration greatly affects band offsets, this would result in a large range of offset values. Other, more probable, options are the measurements do not account for band bending, which may dramatically alter the band-offset values as discussed by Xu *et al.*,[184] or the potential drop across the interfacial oxide layer, which may develop at the interface.

The band offsets of dielectrics on AlGaN and AlN are summarized in Tables VIII[90,141,189–191] and IX,[141,185–188] respectively. For AlGaN, Robertson[141] and Heidelberger[189] determined the theoretical band offsets, using the MIGS Schottky pinning factor and the CNL alignment; however, there are very few experimental results[90,190,191] and none of which that can be compared to the theoretical calculations. Furthermore, it is likely that such investigations on AlGaN will depend heavily on the aluminum content. Therefore, conclusions with regards to the band offsets of dielectrics on AlGaN are less evident at this time.

IV. PROCESSING RELATED EFFECTS

The electronic states may depend on the various processing treatments, such as cleaning, dielectric passivation, postdeposition, and postmetallization treatments. These processing steps may affect states related to oxygen coverage, oxide layers, carbon contamination, structural defects, bonding configurations, vacancy defects, interstitials, absorbates, pinning states, etc. Consequently, understanding how these treatments affect the surface and interface states will aid in the advancement of device technologies.

A. Cleaning and surface processing

Cleaning and processing of GaN and AlGaN surfaces prior to dielectric deposition have proven a critical step in the optimization of device performance. Surface contamination on these materials is commonly related to carbon and oxygen as part of native oxides, absorbates, and residual species. Spectroscopic ellipsometry by Edwards *et al.*[192] has determined that there is ∼2–5 nm of contamination on air-exposed GaN; about half of this contamination consists of transparent inorganic and organic contamination, and the rest is presumed to be native oxide. On AlN and AlGaN surfaces, it is expected that this ratio will vary slightly such that there is more native oxide, since aluminum is more easily oxidized than gallium.[193,194] The goal of cleaning GaN and AlGaN is therefore to remove these contaminants without damaging the crystal order or introducing additional defect states. To accomplish this goal, research has focused on the cleaning of GaN prior to the fabrication of metal/GaN Schottky contacts, using both *ex-situ* and *in-situ* cleaning. *Ex-situ* cleaning has included solvents such as trichloroethylene, acetone, methanol, isopropanol, various acids and bases, as well as

TABLE VIII. Theoretical and experimental band offsets on AlGaN. The deposition method is noted where ECR-CVD = electron cyclotron resonance chemical vapor deposition, MBD = molecular beam deposition, and vap. cooling cond. = vapor cooling condensation. In addition, the characterization method is noted where EELS = electron energy loss spectroscopy, and XPS = x-ray photoelectron spectroscopy. All offsets are given in eV.

				Band offset		
Material	Deposition	Specifics	Characterization	VBO	CBO	Reference
Ga_2O_3		LDA	CNL	0.6[a]	1.4[a]	141, 189
$GdScO_3$		LDA	CNL	−0.2[a]	2.3[a]	141, 189
HfO_2		LDA	CNL	1.6[a]	0.6[a]	141, 189
Sc_2O_3		LDA	CNL	0.8[a]	1.4[a]	141, 189
Si_3N_4		LDA	CNL	0.6[a]	0.9[a]	189
Si_2O_3		LDA	CNL	3.4[a]	1.9[a]	141, 189
Al_2O_3	MBD	Al MBD + ECR plasma	*In-situ* XPS, EELS	0.8	2.1	90
SiN_x	ECR-CVD	$SiH_4 + N_2$	*In-situ* XPS, EELS	0.1	0.7	90
ZnO	Vap. cooling cond,	$TMA + H_2O$	XPS	−1.5	0.8[b]	190, 191

[a]Theoretical value.
[b]Estimated value.

UV/O_3. *In-situ* cleaning has included room temperature or high temperature plasma, sputtering (Ar, Xe, Ne, N_2, H_2, and O_2), and vacuum, or gas (H_2, N_2, NH_3, and Ga flux) annealing as will be discussed below. In most cases, these studies focus on the cleaning of n-type, Ga-face GaN; deviations from this standard will be noted.

1. *Wet chemical cleaning*

Wet chemical cleans have been used to remove native oxides as well as organic and inorganic contamination ever since Hedman and Mårtensson published a study in 1980,[195] showing that submersion in 100 °C H_3PO_4 and *in-situ* annealing at 300 °C reduces oxygen and carbon contamination. More recent research has focused on the effectiveness of several wet chemical cleans; these include hydrochloric acid (HCl), hydrofluoric acid (HF), nitric acid (HNO_3), sulfuric acid (H_2SO_4), phosphoric acid (H_3PO_4), hydrogen peroxide (H_2O_2), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), ammonium fluoride (NH_4F), ammonium sulfide ($(NH_4)_2S$), RCA SC1 and SC2, buffered HF (BHF), and BHF vapor as well as UV/O_3—though not explicitly a wet chemical.

Since contaminants and native oxide consist mostly of carbon and oxygen, most research uses spectroscopy after exposure to various wet chemical cleans to determine their

TABLE IX. Theoretical and experimental band offsets on AlN. Note the experimental band offsets for InN/AlN are given for the Al-face and the N-face, respectively. The deposition method is noted where MOCVD = metal organic chemical vapor deposition, and PEMBD = plasma-enhanced molecular beam deposition. In addition, the characterization method is noted, where XPS = x-ray photoelectron spectroscopy. All offsets are given in eV.

				Band offset		
Material	Deposition	Specifics	Characterization	VBO	CBO	Reference
Al_2O_3		LDA	CNL	3.1[a]	−0.5[a]	141
Ga_2O_3		LDA	CNL	0.7[a]	−2.1[a]	141
Gd_2O_3		LDA	CNL	0.3[a]	−0.7[a]	141
HfO_2		LDA	CNL	1.3[a]	−1.5[a]	141
$HfSiO_4$		LDA	CNL	1.4[a]	−1.1[a]	141
$LaAlO_3$		LDA	CNL	0.9[a]	−1.5[a]	141
La_2O_3		LDA	CNL	0.4[a]	−0.6[a]	141
Sc_2O_3		LDA	CNL	0.3[a]	−0.6	141
Si_3N_4		LDA	CNL	0.4[a]	−1.3[a]	141
SiO_2		LDA	CNL	2.9[a]	−0.1[a]	141
$SrTiO_3$		LDA	CNL	−0.2[a]	−2.7[a]	141
Ta_2O_5		LDA	CNL	0.7[a]	−2.5[a]	141
ZrO_2		LDA	CNL	1.1[a]	−1.5[a]	141
InN	PEMBD	In flux + N_2 plasma	XPS	−1.5	−4.0[b]	185, 186
				−3.1	−2.4[b]	185, 186
MgO	MOCVD	$(Cp_2Mg) + O_2$	XPS	0.2	1.5[b]	187
ZnO	PEMBD	$Zn + O_2$ plasma	XPS	−0.4	−3.3[b]	188

[a]Theoretical value.
[b]Estimated value.

effectiveness. This was the approach taken by Smith *et al.*[196] and King *et al.*,[197] who used Auger electron spectroscopy (AES) and x-ray photoelectron spectroscopy (XPS) to examine the effectiveness of several acids at removing oxygen and carbon from the surface, including HCl, HF, HNO_3, H_2SO_4, H_3PO_4, H_2O_2, NaOH, KOH, NH_4F, RCA SC1 and SC2, BHF, and BHF vapor as well as UV/O_3. Comparative results show that HCl reduces oxygen coverage most effectively, while HF reduces carbon coverage most effectively. (UV/O_3 is shown to be an effective method to remove carbon contamination but only at the expense of further oxidizing the surface.) Furthermore, these acidic cleanings result in very different surface chemistry. For example, HCl-treated samples are characterized by significant chlorine coverage on the surface. The strong bonding between chlorine and gallium or nitrogen and the inverse correlation between chlorine and oxygen on the surface suggest chlorine atoms occupy dangling bonds left by oxygen removal, preventing reoxidation during air exposure.[197,198] XPS also detects two chemical states associated with oxygen, where the core level at higher energy is typically associated with Ga-OH^- bonding, and that at lower energy is associated with Ga-O^{2-} bonding.[197,199–201] However, it has also been suggested that oxygen bonds to nitrogen and forms an oxynitride.[197,200,202] The HF-cleaned samples, on the other hand, show the binding energy of the C 1s core level after HF treatment shifts $\sim$0.4 eV to higher binding energy in comparison with samples after HCl treatment. This shift suggests HF-treated samples are characterized by more C-O bonds, while HCl-treated samples are characterized by more C-H bonds.

Other studies have focused on preventing oxidation and reoxidation. Sulfur-based processes have been successfully used to this end on other semiconductors such as GaAs, because sulfur passivation is hydrophobic and easily removed with low-temperature annealing. Plucinski *et al.*[203] have demonstrated that atomically thin layers of sulfur deposited *in-situ* on a clean Ga adlayer on N-face GaN effectively inhibits oxidation on GaN. Furthermore, similarly sulfur-treated GaN surfaces have been shown to improve ohmic contacts and photoluminescence.[204–206] Sulfur-based wet chemical cleans may induce similar results as shown by Diale *et al.*[207] Their research suggests that, similar to the Cl termination that results from a HCl cleaning, $(NH_4)_2S$ cleaning results in S termination on the surface, which inhibits reoxidation. Consequently, $(NH_4)_2S$-cleaned GaN is characterized by less carbon contamination, reduced oxygen coverage, a smaller RMS roughness, and a better stoichiometric ratio than HCl- or KOH-cleaned GaN. Solutions of sulfuric acid and hydrogen peroxide have also been used with some success on GaN. Nepal *et al.*[208] concluded that H_2O_2:H_2SO_4 (1:5, piranha, 80 °C) cleaning is also more effective than HCl or HF cleaning, giving the best-quality ALD-Al_2O_3/GaN interface in terms of roughness. However, it is unlikely that such a clean would completely remove all oxygen or carbon. This is supported by the work of Machuca and Liu *et al.*,[209,210] who demonstrated that cleaning GaN with a 1:4 H_2O_2:H_2SO_4 at 90 °C reduces oxygen and carbon coverage to $\sim$0.9 ML and 0.7 ML, respectively.

Ammonium hydroxide is another wet chemical clean of interest, which is effective at reducing oxygen but not carbon on GaN and AlGaN surfaces. It is thus suggested that Ga_2O_3 dissolves in NH_4OH,[90,193,211] which likely results in improved device performance. For example, in a study by Koyama *et al.*,[212] results show that pretreatment of GaN in NH_4OH (50 °C) results in better thermionic emission I-V characteristics of Au, Ag, and Pt/GaN Schottky contacts than those treated with HCl or HF. On one hand, these results may be surprising since NH_4OH–cleaned substrates should contain more carbon, which has also been shown to degrade device performance. On the other hand, the acids are not as effective at reducing the native oxide without generating a Ga-rich surface, which ultimately leads to more defects at the interface that are influential to device degradation.

It is also worth mentioning that alkali cleaning on N-face GaN is different from that on Ga-face GaN, where hydroxide solutions such as KOH (Ref. 213) and NaOH (Ref. 214) as well as hot H_3PO_4 (Ref. 215) can selectively etch the N-face GaN, causing morphology degradation. Li *et al.*[213] concluded that selective etching on N-face but not Ga-face GaN is a consequence of different nitrogen surface bonding states. On the N-face, hydroxide attacks the tetrahedrally bonded Ga atoms underneath the terminating N layer, forming Ga_2O_3 and NH_3. The Ga_2O_3 is then dissolved from the surface, leaving a new N-face that can be continuously etched. The Ga-face, on the other hand, is more stable. After Ga_2O_3 is removed from these surfaces, a nitrogen atom on the N-terminated surface is characterized by three occupied dangling bonds, which repel OH^-. There are similar dangling bonds on N-face GaN, which will repel OH^-; however, there is only one dangling bond per nitrogen rather than three. Consequently, OH^- will reach the Ga layer below and cause the etching process (see Fig. 5 for reference).

2. Vacuum annealing

Given that wet chemical treatments cannot completely remove both oxygen and carbon contamination, researchers have looked elsewhere for effective cleaning processes, including *in-situ* annealing. Often these experiments are paired with *ex-situ* chemical cleans, which influence the effectiveness of the annealing. For example, Machuca and Liu *et al.*[209,210] combined the H_2O_2:H_2SO_4 wet chemical clean with an *in-situ* 700 °C vacuum anneal ($\leq 10^{-10}$ Torr), reducing the respective oxygen and carbon coverage from $\sim$0.9 ML and 0.7 ML to 0.08 ML and 0.01 ML. This would suggest that annealing at this temperature may effectively remove carbon but not oxygen. Diale *et al.*[207] also found that additional high temperature vacuum annealing of GaN after chemical treatment results in nearly complete removal of carbon contamination as measured by AES; however, these results also show nearly complete oxygen removal. The more effective cleaning is likely the result of the $(NH_4)_2S$-clean used prior to annealing.

Smith and King *et al.*[196,197] have systematically evaluated the effectiveness of vacuum annealing at various temperatures. Their XPS results show the C 1s core level of

wet-chemical-treated GaN shifts to lower binding energy after annealing at 500–600 °C. This shift suggests that C-O bonding desorbs at this temperature range while C-H bonding requires a higher desorption temperature. This is confirmed by temperature programmed desorption and may explain why thermal desorption of carbon is more effective for HF-treated GaN than HCl-treated—where HF-treated GaN has more C-O bonded carbon remaining as mentioned earlier. Similarly, thermal desorption of Cl occurs at ∼600 °C, while thermal desorption of carbon likely occurs at temperatures above 900 °C. Thermal desorption of surface oxide, however, also becomes significant at temperatures >900 °C. Consequently, vacuum annealing is not an effective method of oxide removal, since sublimation of Ga also occurs at this temperature, which introduces additional defect states.

3. Gas annealing

Similar research has focused on the effects of annealing in gaseous environments, particularly NH_3. King *et al.*[197] have annealed GaN in NH_3 at 800 °C, reducing carbon contamination below the XPS detection limit and leaving only ∼0.1 ML oxygen. A comparable study by Tracy *et al.*[216] has reduced both oxygen and carbon below the detection limit of XPS and ultraviolet photoemission spectroscopy (UPS). Moreover, the Ga/N ratio decreases from 1.3 to 1.0 after annealing, indicating a more favorable stoichiometry. However, other studies were not as successful such as those by Machuca *et al.*[209] and Grabow *et al.*,[217] showing ∼0.48 ML and 0.92 ML oxygen coverage, respectively. It is likely that this discrepancy is related to the substrate growth or annealing conditions; at high temperatures, the purity of the ultra high vacuum chamber and annealing gas plays a crucial role in the effectiveness of NH_3 annealing. High-temperature NH_3 annealing has also been combined with N_2^+ ion bombardment and deposition of Ga metal by Bermudez *et al.*[223] This study found that annealing ≤900 °C in NH_3 is only effective at removing carbon not oxygen. They proposed that oxygen at subsurface sites or in the form of Ga_2O_3 is inaccessible to NH_3 and thus requires annealing in NH_3 at temperatures >900 °C for removal.

4. Ion sputtering and annealing in flux

In some cases, ion sputtering has proven a useful method in optimizing stoichiometry during cleaning. To date, several ions have been considered, including Ar^+,[218–220] Xe^+,[218] N_2^+,[218–221] and Ne^+.[219] In some of these cases, namely Ar^+, Xe^+, and Ne^+, sputtering causes defect formation with the preferential removal of nitrogen, forming metallic Ga clusters with subsequent annealing above 350 °C.[218] In contrast, N_2^+ sputtering barely decreases the N/Ga ratio, and postannealing further increases that ratio to near unity. It is also suggested that N_2^+ sputtering helps generate not only a stoichiometric but also an ordered GaN (1×1) surface.[218,219,221]

Annealing in a flux of Ga is another suitable method of contamination removal that maintains stoichiometry and may be more effective at reducing defect formation. Work by Asif Kahn *et al.*[222] demonstrated that this method can achieve atomically clean GaN after exposure to $\sim 5 \times 10^{15}$ cm^{-2} min^{-1} Ga flux at 900 °C, while effectively removing carbon contamination; *in-situ* AES results show the intensity ratio of C KLL to N KLL is below 0.02, while oxygen contamination is close to the AES sensitivity limit. In a similar study, Bermudez *et al.*[223,224] cleaned GaN by depositing Ga metal on the sample surface followed by annealing in UHV at 900–950 °C. The carbon and oxygen contamination is reduced below the AES sensitivity limit (>0.01 and 0.005 ML, respectively). As an alternative method, Bermudez[201] applied N_2^+ sputtering on GaN followed by 900 °C UHV annealing to achieve similar contaminant reduction below the sensitivity limit of AES, suggesting that N_2^+ sputtering prior to annealing may help prevent the formation of N vacancies that occur during UHV annealing.[225] Both Ga and N_2^+ sputtering yield (1×1) ordered surfaces.

5. Plasma annealing

In many cases, annealing in plasma, particularly H_2 and N_2 plasma, is more effective at removing contaminants than other methods at lower temperatures because of the reactivity of the plasma species. This has been shown by King *et al.*;[197] they found H_2 plasma can remove carbon and halogens at 450 °C, which is much lower than the temperature needed to remove these contaminants in the vacuum, NH_3, or Ga flux. Combination with N_2 plasma makes the cleaning even more effective as shown by Yang *et al.*,[111] who compared cleaning processes of H_2, N_2, and H_2/N_2 (1:4) plasma at 650 °C. Moreover, N_2 plasma annealing at 700–750 °C is a more effective method at removing carbon contamination than Ga deposition/readsorption as demonstrated by Schulz *et al.*,[226] though deposition/readsorption is a more efficient method of oxygen removal. Both methods result in clear (1×1) LEED patterns. These results suggest that plasma annealing is a comparatively effective means of reducing carbon.

Many studies have also investigated the effectiveness of plasma annealing at removing oxygen. For example, after removing carbon contamination *ex-situ* with HCl and UV/O_3, Lee *et al.*[227] investigated the effects of N_2 and N_2/H_2 plasma at removing oxygen from GaN at 750 °C or 900 °C. At both temperatures, both carbon and oxygen are below the limit of AES sensitivity; however, a large amount of surface oxygen (2×10^{22} cm^{-3}) and carbon (3×10^{20} cm^{-3}) is still measured on GaN by secondary ion mass spectroscopy. Hashizume and Inagaki *et al.*[90,228,229] reported that electron cyclotron resonance (ECR) H_2 and N_2 plasma at 280 °C is effective at significantly reducing but not eliminating oxygen and carbon from AlGaN. Furthermore, the samples cleaned with H_2 plasma are characterized by a decrease in the N signal as measure by XPS, suggesting that H_2 plasma reacts with the surface to form volatile NH_x groups. This may cause N-vacancy related defects, or metallic Ga and/or Al on the surface, degrading device performance. The N_2 plasma is thus believed to suppress the formation of N vacancies. Jin and Hashizume *et al.*,[228,230] using dry etching with ECR $CH_4/H_2/$Ar plasma, have also suggested this hypothesis.

Similar studies have shown that plasma cleaning can improve reliability issues and device performance. Meyer

et al.[231] demonstrated that SF_6- and/or O_2- plasma cleaned SiN_x/AlGaN/GaN HEMTs achieve better current collapse characteristics than untreated or wet chemical treated devices, which is likely connected to their relative effectiveness at removing carbon from AlGaN. Similarly, Guhel *et al.*[232] used O_2 plasma to remove carbon and/or CF_4 plasma to remove oxygen, where the largest drain current and smallest knee voltages where obtained using the combined ($O_2 + CF_4$) pretreatment. It is thus observed that this pretreatment may decrease the influence of electrical traps located at the AlGaN surface. Hoshi *et al.*[233] reported that an optimized NH_3 plasma can remove carbon contamination and suppress current collapse in SiN_x/AlGaN/GaN HEMTs; however, an extended NH_3 plasma process may degrade the stoichiometric composition of the AlGaN surface and impact current collapse suppression. Kim *et al.*[234] have suggested that NH_3 plasma may introduce interstitial H^+, which passivates bulk defects and explains the lower current collapse in NH_3-plasma treated AlGaN/GaN HEMTs compared to N_2-plasma treated. This is supported by the work of Hierro *et al.*,[235] who maintain that hydrogen can passivate bulk defects in n-type GaN through plasma processing. They propose that although the formation energy of H^+ is higher than that of H^- in n-type GaN,[236] H^+ can diffuse deeper into GaN to passivate the deep level defects due to a lower migration barrier.[236] It may also be worth mentioning that the effects in p-type GaN may be different, where the incorporation of hydrogen can form a Mg-H complex. Therefore, as Nakamura *et al.*[237] reported the resistivity of p-type GaN annealed in NH_3 above 400 °C significantly increases. This ultimately leads to degradation of the carrier concentration in p-type GaN and reduced device performance.[237–239]

6. ALD precursor cleaning

ALD is a chemical vapor deposition (CVD) technique which uses a self-limiting gas-phase chemical process and consequently generates uniform and conformal thin films.[240] One cycle of ALD growth consists of four steps: first, a self-limiting reaction between the substrate and the first reactant or precursor; second, a purge step to remove non-reacted precursor and gaseous by-products of the reaction; third, a self-limiting reaction between the second reactant and the first reactant absorbed on the surface; and lastly, another purge step.[241] This gives a growth rate in terms of growth per cycle, typically 0.5–1 Å. Consequently, the thickness of the film can be precisely controlled, giving uniform and conformal films.

This series of chemistry driven half-cycles can be employed in cleaning as well as deposition. In the ALD deposition of Al_2O_3, the reactants used are most commonly trimethylaluminum (TMA) and H_2O. Experiments on GaAs (Ref. 242) and InGaAs (Ref. 243) show that the first TMA pulse removes the trivalent oxides of gallium and arsenic. It has been suggest that the removal is associated with a ligand exchange mechanism between TMA and the native oxide, where the Al^{3+} ion in $Al(CH_3)_3$ preferentially replace As^{3+} and Ga^{3+} in the related oxide, forming AlO_x and volatile $As(CH_3)_3$ and $Ga(CH_3)_3$.[244,245] Similar studies have been applied to GaN with less success. One study by Sivasubramani *et al.*[202] shows no significant reduction of Ga-oxide after the first TMA half cycle. In another study by Liu *et al.*,[246] results show that a H_2O pretreatment results in fewer interface traps as will be discussed later.

7. Summary

In summary, there has been much progress on cleaning GaN and AlGaN with *ex- and in-situ* processes. In terms of *ex-situ* processes, cleaning with UV/O_3 and HF are most effective at removing carbon contamination for both GaN and AlGaN, while HCl, HF, NH_4OH, and $(NH_4)_2S$ are most effective at removing oxygen. In some of these cases, the wet chemical leaves Cl- or S-termination, which inhibits surface reoxidation. The *p*H and oxide-reduction potential of the selected etchant are also crucial to obtaining an oxide-free and balanced-stoichiometry surface.[247] However, complete contamination removal has not been achieved by *ex-situ* cleaning methods alone. Further *in-situ* treatments, such as Ga deposition/readsorption or N_2^+ sputtering along with high temperature annealing, are more likely to be effective at removing carbon and oxygen. Additionally, H_2/N_2 and NH_3 gas and/or plasma may be more efficient at passivating the surface and bulk defects. The polarization of the substrate may be a factor as well because of the stability of various bonding; namely, the Ga-face is more stable than N-face in hydroxide solutions and hot H_3PO_4. It is also likely that the magnitude of the polarization will affect the cleaning, where increasing the polarization is achieved by increasing the aluminum content and altering the surface chemistry.

Ultimately, these cleans will have a profound effect on device performance, where the cleaning requirements vary with the specifics of the desired device. For example, cleaning requirements for metal/GaN interfaces may be different from that for gate dielectric/GaN. For example, residual Cl and S on the GaN surface may enhance the adhesion of metals and improve device performance. Similarly, plasma or ion sputtering can improve the ohmic contact properties of metal/GaN by causing point defects such as donor-like nitrogen vacancies, which may create a thin n-type layer between the metal and GaN. However, for dielectric/GaN interfaces, these vacancies may induce electrically active defects at the interface or in the dielectric, degrading the device. In other words, understanding interface electronic states is even more complicated as it must integrate the results of various surface treatments, dielectric properties and growth methods, metal contacts, and device behavior.

B. Dielectric passivation and interface processing

Device behavior can also be modified with the incorporation of dielectrics, which are typically used to mitigate reliability issues in one of two ways: as a gate dielectric and as a passivation layer. The distinction between these two functions is not typically emphasized since the dielectric often functions as both. However, there are some cases where different dielectrics are employed for each component. Thus, for clarity, the two are distinguished by their position in the

device, where the gate dielectric is the material underneath the gate, which mitigates gate leakage, and the channel passivation layer is the material between the gate and the drain, which mitigates current collapse. The device characteristics will therefore depend critically on the dielectric properties; the two most important being the band gap and the dielectric constant, where one determines the confinement characteristics of the carriers and the other relates to the electric field across the dielectric. Ideally, a gate insulator would have a large band gap and a large dielectric constant, resulting in large band offsets that permit carrier confinement and large capacitance that permits device scaling; however, the two properties are often inversely related. There are other factors to consider as well, such as the crystal structure of the dielectric. In many cases, amorphous materials are preferred to crystalline, since crystalline materials may be characterized by grain boundaries. These defects serve as tunneling paths or tapping states and thus mitigate the effectiveness of the dielectric. Single crystal structures, on the other hand, may be promising but often require high temperature deposition as well as consideration of the lattice mismatch between the semiconductor and insulator. If this parameter is not optimized, it may result in a high concentration of structural defects at the interface. Furthermore, the deposition method and material type may alter the defect concentration at the interface or in the insulator, which affect trap-assisted tunneling processes. Additionally, the thermal and chemical properties must be considered when evaluating an insulator. In other words, there are several parameters to be considered when evaluating the effectiveness of a dielectric.

To date, a number of dielectrics have been considered for passivation layers and gate dielectrics on GaN and AlGaN devices. Section IV A 1 will give a detailed discussion of recent research, which considers various dielectrics, including silicon oxide (SiO_2), silicon nitride (SiN_x), aluminum nitride (AlN), low-temperature gallium nitride (GaN), gallium oxide (Ga_2O_3), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), titanium oxide (TiO_2), scandium oxide (Sc_2O_3), magnesium oxide (MgO), calcium oxide (CaO), lanthanum oxide (La_2O_3), lutetium oxide (Lu_2O_3), gadolinium oxide (Gd_2O_3), tantalum oxide (Ta_2O_3), zinc oxide (ZnO), and praseodymium oxide (Pr_2O_3). There are other dielectrics that have been considered as well, but these represent the most prominently used in GaN-based studies.

For clarity, it should be noted that comparing the performance of these dielectrics can be potentially problematic since surface pretreatments, dielectric deposition, device fabrication, and postdeposition treatments are not consistent between different studies. Additionally, studies that report the interface trap density (D_{it}) conventionally describe the minimum measured value, which is not necessarily representative of the distribution of states across the band gap and may not even represent the actual minimum value, depending on the range of the probing technique. For simplicity, this convention is continued in Sec. IV B 1, but it should be kept in mind that these values may be misleading.

1. SiO_2 and SiN_x

On GaN and AlGaN, the most extensively researched dielectrics are SiO_2 and SiN_x,[47,50,85,90,248–253] which have been considered both as gate insulators and channel passivation layers. Their appeal is largely related to their current widespread use in Si-based technologies, and thus they are well-understood materials. Furthermore, they have been proven effective at reducing leakage current by ~4 orders of magnitude and increasing the gate voltage that results in current collapse in MOSHFETs and MISFETs (metal-insulator-semiconductor heterostructure field-effect transistors).[47,48,51]

Comparatively, SiN_x is a better dielectric in terms of the dielectric constant (~7.5) at the expense of the band gap (~5.0 eV). Additionally, SiN_x may be advantageous because it is unlikely to oxidize the substrate during dielectric deposition like SiO_2 and may passivate nitrogen-vacancy related defects on the surface during dielectric growth. Ultimately, this should result in a lower D_{it}. For example, using ECR-PECVD SiN_x, Nakasaki *et al.*[180] measured the D_{it} of SiN_x/GaN to be 5×10^{10} $cm^{-2} eV^{-1}$, after NH_4OH wet-chemical and N_2-plasma pretreatments. Alternatively, using RF-PECVD SiO_2, they measured the D_{it} of SiO_2/GaN to be $3 \times 10^{11} cm^{-2} eV^{-1}$, after the same wet chemical pretreatment. In other words, the D_{it} of SiN_x/GaN is ~6 times lower than the D_{it} of SiO_2/GaN. On the other hand, the D_{it} is sensitive to the processing and deposition conditions, and therefore, there are cases where SiO_2/GaN interfaces will have a lower D_{it} than SiN_x/GaN. In a study by Arulkumaran *et al.*,[254] the D_{it} is compared for e-beam SiO_2, PECVD SiO_2, and PECVD SiN_x in GaN MIS devices; their respective D_{it} were 5.3×10^{11}, 2.5×10^{11}, and $6.5 \times 10^{11} cm^{-2} eV^{-1}$. In this case, PECVD-deposited SiO_2 has a smaller concentration of interface traps than similarly grown SiN_x. Similarly, Bae *et al.*[250] reported not only a lower D_{it} and electron trapping but also a lower leakage current and improved reproducibility properties for SiO_2/nitrided-thin-Ga_2O_3/GaN ($D_{it} = 4 \times 10^{11} cm^{-2} eV^{-1}$) relative to SiN_x/GaN ($D_{it} = 9 \times 10^{11} cm^{-2} eV^{-1}$). Moreover, in terms of current collapse, ALD-deposited SiO_2 (Refs. 47, 248, and 251) is comparable to PECVD SiN_x (Ref. 252) passivation on AlGaN/GaN HFETs.

Combinations of SiO_2 or SiN_x have also been tried as passivation layers and/or gate insulators because of the reciprocal nature of the dielectric constants and band gaps of these materials; as mentioned, SiO_2 has a smaller dielectric constant (3.9) but a larger band gap (8.9 eV) than SiN_x. Therefore, an alloy such as SiON should have an intermediate dielectric constant (3.9–7.5 eV) and band gap (5.0–9.0), which depend on the stoichiometry of the film. One such alloy has been studied on HEMTs by Arulkumaran *et al.*[255] and Balachander *et al.*[256] Their results show that SiON not only reduces the gate leakage current by four orders of magnitude in comparison to unpassivated devices but also reduces current collapse and hysteresis width in comparison to SiN_x-passivated HEMTs. Similarly, stacked SiN_x/SiO_2 structures have been employed. In these studies, Balachander *et al.*[257] have illustrated that SiN_x/SiO_2-passivated AlGaN/GaN HEMTs have a slightly lower current collapse and a higher leakage current

compared to SiO_2-passivated devices as well as a lower leakage current and a slightly higher current collapse compared with SiN_x-passivated devices. In another study by Lachab *et al.*,[50] the gate dielectric and channel passivation dielectric are differentiated; 4.2 nm SiO_2 is used as the gate insulator, and 30 nm SiN_x is used as the channel passivation layer. Results show that separating the two successfully suppresses the leakage current and current collapse.

2. Other nitrides

In addition to SiN_x, other nitrides, namely AlN, have been studied as a gate dielectric and/or passivation layer. AlN has a small mismatch with respect to GaN (~0.3%),[258] which may minimize strain-induced defects at the interface depending on the deposition method. For example, sputtered AlN on AlGaN/GaN heterostructures has been compared to e-beam SiO_2 and PECVD SiN_x by Chen *et al.*[259] Of these three heterostructures, the AlN-passivated has the highest 2DEG mobility and a higher 2DEG density than SiO_2-passivated and unpassivated structures—though not SiN_x-passivated. Furthermore, high-temperature strain-relaxation is also best optimized for AlN.[260] On the other hand, high energy sputtering may cause surface damage and ultimately limit the performance and reliability of the device. Consequently, other deposition methods have been considered as well. In MOCVD-grown AlN/GaN MIS structures, Hashizume *et al.*[261] measured a low D_{it} ($<1 \times 10^{11}\,cm^{-2}\,eV^{-1}$), and in ALD-AlN/AlGaN/GaN HEMTs, Huang *et al.*[262] have shown an atomically sharp interface between AlN and AlGaN as well as significant reduction in current collapse and dynamic on-resistance.

Low-temperature GaN has also been investigated as a potential gate insulator. On one hand, it may be counterintuitive to consider GaN a gate dielectric; however, the distinction is that dielectric GaN is grown at low temperature. Low-temperature-grown GaN has very different qualities than high-temperature-grown GaN, namely a poor crystalline quality and very high resistivity.[263] It may therefore be advantageous as a dielectric given the small lattice mismatch. Furthermore, deposition can be done *in-situ* after growth, which limits contamination. For these reasons, Kao *et al.*[264] have considered low-temperature, GaN-passivated AlGaN/GaN HFETs in comparison with SiO_2 and SiN_x-passivated devices. Their results show that GaN may be a better gate dielectric than SiO_2 or SiN_x, giving the highest sheet carrier concentration (~50% higher than that of unpassivated HFET) and reduction in current collapse because of the superior lattice match. On the other hand, the band gap of GaN is small with insignificant band offsets, and therefore, GaN may not be as effective at limiting the leakage current.

3. Gallium oxide

Ga_2O_3 is also of interest as a gate dielectric and passivation layer for GaN and AlGaN MOS devices, with a band gap of 4.8 eV and dielectric constant of 10.2–14.2. One of the benefits of Ga_2O_3 is that it can be natively grown on GaN via thermal and chemical process, which can limit contamination at the interface.[265,266] Unfortunately, thermal oxidization is extremely slow for temperatures <800 °C,[199] and higher temperatures may cause surface damage as previously mentioned. Lee *et al.*[266] circumvented this issue by oxidizing GaN in a H_3PO_4 solution with a *p*H value of 3.5 and laser illumination. This oxidation process achieves a D_{it} of $2.5 \times 10^{11}\ cm^{-2}\,eV^{-1}$ with a reasonable leakage current (6×10^{-7} A/cm^{-2} at −20 V) and reasonable forward and reverse breakdown field (2.80 MV/cm and 5.70 MV/cm, respectively). However, the relatively small band gap of 4.8 eV of Ga_2O_3 cannot effectively suppress the leakage current. Moreover, Ga_2O_3 is also difficult to grow on AlGaN, where aluminum is more easily oxidized than gallium.

4. Aluminum oxide

Amorphous Al_2O_3 (Refs. 88, 267–269) has been favored by many studies because of the large band gap (~7 eV), sufficient dielectric constant (~10), high breakdown field (10 MV/cm), high thermal (<850 °C) and chemical stability on AlGaN. Hashizume *et al.*[90] demonstrated MBE-grown, Al_2O_3-passivated AlGaN/GaN is characterized by good control of drain current up to $V_{GS} = +3$ V, no current collapse under the quiescent gate voltage stress, and lower leakage current at forward bias compared to SiN_x-passivation. This is likely a result of the larger conduction band offset of Al_2O_3. ALD-grown Al_2O_3 has also shown some favorable results by Park *et al.*[267] and Chang *et al.*,[269] the latter calculating a D_{it} of (4–9) $\times 10^{11}\ cm^{-2}\,eV^{-1}$. As mentioned, ALD results may vary depending on the deposition conditions; Liu *et al.*[246] found that pretreatment with H_2O prior to ALD growth yields an extremely low D_{it} (~$2 \times 10^{10}\,cm^{-2}\,eV^{-1}$). In other words, Al_2O_3 exhibits excellent performance in suppressing gate leakage and current collapse in GaN-based devices; this dielectric has a lower D_{it} by an order of magnitude, a higher dielectric constant, and similar gate leakage suppression compared to reports of Si-based dielectrics. However, the dielectric constant of Al_2O_3 is still relatively low in comparison with other materials, and thus, Al_2O_3-passivated devices may also be characterized by a less than optimal threshold voltage shift and decrease in transconductance. It may therefore be advantageous to use Al_2O_3 as an interfacial passivation layer with a higher dielectric constant film, such as HfO_2.[270]

5. Hafnium and related oxides

Amorphous hafnium and related oxides have shown significant promise because of their high dielectric constants (~20–25) (Ref. 271) and sufficient band gaps (5.8 eV). For this reason, HfO_2 is currently used to replace SiO_2 as the gate insulator in Si-based MOSFET fabrication, which allows for device scaling. HfO_2 is, therefore, likely to effectively diminish the gate leakage in GaN-based MOSFETs as well. Liu *et al.*[175] demonstrated that this is indeed the case, where sputtered HfO_2 reduces the leakage current by five orders of magnitude from unpassivated HEMTs. This work also shows that HfO_2 reduces current collapse, increases gate voltage swing, and augments cut off frequencies. Furthermore, HfO_2-based devices exhibit only a small reduction in transconductance because of the relatively high-k dielectric constant. Another

study of ALD-HfO_2/GaN by Chang *et al.*[271] reveals a D_{it} of 2×10^{11} $cm^{-2} eV^{-1}$ in addition to negligible current collapse and a low leakage current density (10^{-7}–10^{-8} A/cm^2 at 1 MV/cm).

On the other hand, HfO_2 is less thermally and chemically stable than Al_2O_3, where amorphous HfO_2 crystallizes into predominantly monoclinic polycrystalline films on Si at only 300–500 °C.[272,273] This is disadvantageous as crystalline structures are more likely to contain grain boundaries, which enhance leakage. Consequently, in an attempt to combine the stability and larger band gap of Al_2O_3 with the large dielectric constant of HfO_2, there have been several investigations into stacked HfO_2/Al_2O_3 as well as HfAlO alloys. For example, Yue *et al.*[270] fabricated a HfO_2/Al_2O_3-passivated AlGaN/GaN MOSHEMTs using ALD. Their device had no measureable C-V hysteresis, a small threshold voltage shift, a maximum drain current of 0.8 A/mm, a peak g_s of 150 mS/mm, and leakage current at least six orders of magnitude smaller than an unpassivated HEMT. Furthermore, as long as the device surface was properly passivated, the device did not show current collapse; a single layer of Al_2O_3 could adequately suppresses current collapse, and additional HfO_2 layers more effectively reduced the leakage current. In addition to the stacked structure, Liu *et al.*[246] have also investigated MOCVD HfAlO (10% Al) to achieve a higher stability and crystallization temperature with respect to HfO_2 and higher dielectric constant with respect to Al_2O_3. Results give a D_{it} between 7.8×10^{10} and 2.38×10^{10} $cm^{-2} eV^{-1}$, depending on the pre-deposition surface processing.

Other related high-k materials comparable to HfO_2 have also been considered, such as ZrO_2 with a band gap of ~5.8 eV and dielectric constant of ~20 as well as TiO_2 with a band gap of 3.2 eV and a dielectric constant of ~24–96, depending on the TiO_2 film phase.[274] ZrO_2/GaN HEMTs have been studied by Balachander *et al.*[275] In these devices, the maximum current density (1.17 A/mm) is twice that of unpassivated devices, and the leakage current is four orders of magnitude lower. It appears thus that ZrO_2 may still be less effective than HfO_2 in this regard, though it is difficult to ascertain without a more direct comparison. Other studies by Hu *et al.*[276] on GaN MOSHEMTs with TiO_2 as a gate insulator and passivation layer show the device is characterized by twice the maximum drain current (0.84 A/mm), a higher breakdown field (13 MV/cm), a decreased D_{it} (6.4×10^{11} $cm^{-2} eV^{-1}$), and a significantly suppressed current collapse. Furthermore, the leakage current in reverse bias (~5.1×10^{-9} A/cm^2 at 1 MV/cm) is comparable to other high-k materials; however, given the small band gap of TiO_2, it may further benefit from an additional higher band-gap dielectric capping layer. Similar to the combination of HfO_2 and Al_2O_3 or SiO_2 and SiN_x, the stacked structure would augment the overall band gap of the combined dielectric, though slightly compromising the high-k benefits.

6. Scandium and magnesium oxides

Sc_2O_3 has a sufficient band gap of 6.3 eV, high dielectric constant of ~14, and a lattice mismatch of ~9% for cubic bixbyite crystalline films, such that the (111) orientation is parallel to (0001) GaN. This orientation has been obtained via MBE deposition in several reports,[277–279] which consider heteroepitaxy as beneficial to the electrical properties. In particular, these studies argue that epitaxial dielectrics may minimize the density of surface states, by occupying surface dangling bonds on the substrate. On the other hand, MBE may not yet be readily scalable for high-yield manufacturing. Therefore, Wang *et al.*[280] have also investigated the performance of ALD Sc_2O_3 thin films on AlGaN/GaN devices, which result in a polycrystalline dielectric film with some misoriented grains. This group suggested that these devices have excellent electrical properties such as high I_{on}/I_{off} ratio and low subthreshold slope. Mehandru *et al.*[281] also determined that Sc_2O_3 is efficient at reducing current collapse, where Sc_2O_3-passivated devices were characterized by ~40% less current collapse than unpassivated devices. Furthermore, the effectiveness of Sc_2O_3 passivation is not strongly affected by high-energy (40 MeV) proton irradiation and thus may be of interest in environments with high fluxes of ionizing radiation.[282]

MgO has also been considered as a gate passivation layer and gate insulator with a large band gap (8.0 eV), sufficient dielectric constant (~10), and small lattice mismatch (−6.5%), where Sc_2O_3 and MgO both effectively suppress the current collapse in AlGaN/GaN HEMTs and have a respective D_{it} of 5×10^{11} and 2×10^{11} $cm^{-2} eV^{-11}$, as shown by Luo *et al.*[283] Furthermore, they suggest that these dielectrics may be advantageous over SiN_x with regards to long-term device stability because of the smaller hydrogen content in the films, though comparative studies have not yet confirmed this. In other words, Sc_2O_3 and MgO are effective passivation layers with slightly different advantages; MgO may be more effective as a gate dielectric given its larger band gap while Sc_2O_3 is more chemically stable and less likely to oxidize. Polyakov *et al.*[284] have therefore investigated MgScO/GaN relative to Sc_2O_3 and MgO/GaN in an attempt to take better advantage of these properties. The result is a lower D_{it} at the MgScO/GaN interface (~1×10^{11} $cm^{-2} eV^{-1}$) than either Sc_2O_3/GaN or MgO/GaN.

The lattice mismatch of MgO can be further decreased with a magnesium calcium alloy, forming crystalline Mg_xCa_yO as shown by Gila *et al.*[285] Depending on the composition, the lattice mismatch varies from −6.5 to 6.9 eV, where $Mg_{0.5}Ca_{0.5}O$ is the lowest (−0.23%) of the compositions studied. It may be possible to further decrease the lattice mismatch with a slightly different composition. However, while MgCaO is more stable than MgO, it does not exhibit the stability required for optimal device performance. The research, therefore, suggests the addition of a Sc_2O_3 capping layer.

7. Rare earth oxides

In addition to Sc_2O_3, rare earth oxides have also been considered as a device dielectric because of their high dielectric values and thermal stability. La_2O_3 is one such material, with a large dielectric constant (18–27) and sufficient band gap

(4.3–6.4 eV), depending on the crystal structure; for cubic, the dielectric constant is 18, and for hexagonal, the dielectric constant is 27. The high dielectric constant suggests it would improve device transconductance; however, La_2O_3/GaN is also characterized by a large lattice mismatch (∼20%), and therefore has a larger D_{it} and leakage current than Sc_2O_3/GaN devices.[279] Work by Chiu *et al.*[286] has also suggested that La_2O_3 is not effective at mitigating gate leakage, where La_2O_3-passivated AlGaN/GaN HEMTs reduce the leakage current by only one order of magnitude relative to unpassivated devices. Furthermore, this material is also hygroscopic, which is unfavorable to device performance. La_2O_3 may, therefore, be a favorable constituent in an alloyed dielectric. In one such study, Yang *et al.*[287] alloyed La_2O_3 with Lu_2O_3, fabricating LaLuO-passivated MOSHEMTs. Lu_2O_3 has a large band gap with better hygroscopic immunity but a lower dielectric constant and crystallization temperature. Therefore, the alloy should increase the hygroscopic immunity and band gap at the expense of the thermal stability and dielectric constant. Device characterization shows a leakage current lower than the unpassivated devices with a reasonable maximum drain current (0.82 A/mm at a gate bias of +3 V) and a high transconductance (∼192 mS/mm).

Gd_2O_3 is another rare earth oxide that has been considered, where the dielectric constant (11.4) and band gap (5.3 eV) are sufficient. Similar to Sc_2O_3, Gd_2O_3 is characterized by a bixbyite crystalline structure and grows with the (111) plane parallel to (0001) GaN; however, Gd_2O_3 has a much larger lattice mismatch (∼20%), which results in a larger D_{it} and interface roughness in dielectric/GaN MOSFETs as shown by Gila *et al.*[288] On the other hand, this dielectric has still been characterized by a sufficiently low D_{it} as shown by Das *et al.*,[289] where single crystal Gd_2O_3 has been deposited on HCl-cleaned AlGaN/GaN heterostructures and has a D_{it} of $1–3 \times 10^{11}$ cm^{-2} eV^{-1}. However, the leakage current for single crystal Gd_2O_3/GaN MOS capacitors as measured by Chang *et al.*[290] was mediocre (4.6×10^{-6} mA/cm^2) with small current collapse and hysteresis. Given the large lattice mismatch, mediocre dielectric constant, and adequate band gap, it seems unlikely that Gd_2O_3 could surpass other dielectrics on similar devices. It may, therefore, be beneficial to consider Gd_2O_3 in conjunction with another dielectric such as SiO_2. In another study, Johnson *et al.*[291,292] fabricated Gd_2O_3/GaN-based MOSFETs with an additional SiO_2 layer between the gate and Gd_2O_3 to further reduce the leakage current and increase the breakdown field. In other words, crystalline Gd_2O_3 is a mediocre dielectric in terms of mitigating reliability issues because of the large lattice mismatch but an advantageous dielectric in terms of the thermal stability on GaN (<1100 °C).[290] It may, therefore, be that this dielectric is more successful as an amorphous film, such as $Ga_2O_3(Gd_2O_3)$, which has demonstrated high thermal stability <800–900 °C on InGaAs.[293,294] In a study by Ren *et al.*,[295] e-beam amorphous $Ga_2O_3(Gd_2O_3)$/GaN MOSFETs are characterized by a significantly reduced gate leakage current at elevated temperature relative to unpassivated devices. In fact for these MOSFETs, device operation improved at increased temperatures <400 °C.

8. Zinc and miscellaneous oxides

Other dielectrics, such as ZnO (Refs. 190, 296, and 297) have been considered as gate insulators and/or passivation layers on GaN and AlGaN/GaN-based devices. In particular, ZnO is very similar to GaN, with the same crystal structure, a similar band gap, and small lattice mismatch. Chiou *et al.*[190,191] have shown that this dielectric can be used to improve the interface quality of AlGaN/GaN HEMTs. Additional surface processing such as $(NH_4)_2S$ or HCl treatments may further improve the quality of the interface by reducing the surface states with the formation of Ga-S and Ga-Cl bonds on the AlGaN surface. Consequently, these devices have a reduced current collapse relative to unpassivated AlGaN/GaN MOSHEMTs. However, given its small band gap (3.4 eV), it is unlikely that ZnO will be an effective gate dielectric and may benefit from a stacked or alloyed structure.

Ta_2O_5 is another transparent oxide with a large dielectric constant (∼25) but a relatively small band gap (4.4 eV). In particular, this dielectric has shown some benefits over traditional dielectrics. Wang *et al.*[298] investigated variations in the 2DEG carrier concentration of AlGaN/GaN structures passivated with MOCVD Ta_2O_5 relative to SiO_2, Al_2O_3, and Si_3N_4. Their results show that for thin Ta_2O_5 films (2–4 nm) the 2DEG increases but decreases for thicker films (>4 nm). This behavior suggests that there is positive charge at the Ta_2O_5/AlGaN interface but the majority of charge in the bulk is fixed and negative. Therefore as the oxide thickness increases, the number of negative charges increases, reducing the 2DEG. The 2DEG concentration of SiN_x-passivated structures, on the other hand, increases with thickness. The authors suggest that this may be related to an increase in the piezoelectric polarization charge due to strain. In another comparative study of ALD dielectrics on AlN/GaN HEMTs, Deen *et al.*[299] compared the effectiveness of Ta_2O_5 relative to HfO_2, showing that Ta_2O_5 may give better device performance. Ta_2O_5-passivated devices have a smaller surface roughness and D_{it} ($2–4 \times 10^{13}$ cm^{-2} eV^{-1}) than HfO_2-passivated devices (10^{13} cm^{-2} eV^{-1}) as well as a greatly improved transconductance, which is likely related to a higher dielectric constant. Furthermore, despite the lower band gap, the Ta_2O_5 structures are characterized by a comparable gate leakage current. This research would suggest that thin Ta_2O_5 might prove advantageous.

Other oxides, such as Pr_2O_3,[300] may also prove influential in the development of GaN-based devices; this review has provided an overview of some of the most promising to date, though is by no means comprehensive.

9. Summary

In summary, there have been some significant strides in mitigating reliability issues with dielectric passivation schemes and gate dielectrics, but there is still no perfect solution. The complexity of this issue is intricately linked to the reciprocal nature of the dielectric constant and band gap and may also be related to the different mechanisms responsible for gate leakage and current collapse. For examples, since current collapse is associated with defects at the

AlGaN or GaN surfaces, the most likely cause may be either nitrogen vacancies or electric field driven oxidation from atmospheric moisture. Therefore, the most effective dielectrics at mitigating this mechanism are nitrides, such as SiN_2, AlN, and even GaN, as most experimental studies demonstrate. In addition, nitride passivation increases the 2DEG concentration in AlGaN/GaN structures. On the other hand, the band gap of the nitrides is smaller than many of the oxides, making them less effective at reducing the leakage current. Therefore, N_2 plasma treated oxides could come to play an integral role in future devices; N_2 plasma influences the passivation of nitrogen vacancies or the nitridation of the dielectric. Either mechanism might explain the success of Al_2O_3 with N_2 plasma processing.

Al_2O_3 remains one of the more competitive dielectrics given the large band gap, thermal and chemical stability. On the other hand, Al_2O_3 has a lower dielectric constant and thus a lower transconductance. Consequently, Al_2O_3 may be better as an interfacial passivation layer with a higher dielectric material, such as HfO_2, ZrO_2, or even Ta_2O_5. However, these oxides also have a concentration of negative bulk charge, which may correspond to oxygen-related defects. This charge could decrease the 2DEG carrier concentration and aid in leakage current. It is also worth noting that native oxides are not yet an effective means of passivation, and given the large number of defects that are created after electrical stressing, it may prove crucial to remove the native oxides prior to deposition.

There has also been some success with epitaxial dielectric passivation schemes and gate oxides. It is suggested that these dielectrics will decrease the D_{it} given the small lattice mismatch with Sc_2O_3, MgO, and CaO. However, while there is no direct comparison, experiments have obtained similar D_{it} and interface qualities with amorphous films as well. It, therefore, seems unlikely that epitaxial films will be advantageous to the advancement of GaN-based devices. Amorphous films can be deposited at lower temperatures and are not as likely to crystallize, which may help to prevent the formation of defects with associated gate leakage mechanisms such as trap-assisted tunneling or Frenkel–Poole emission.

C. Postdeposition and postmetallization processing

Given the success of N_2 plasma treatments, other attempts to passivate surface states have focused on postdeposition and postmetallization techniques, which have been shown to reduce the deep-level traps and interface states.[14,114,301–304] For example, Edwards *et al.*[305] report that after dielectric deposition, NH_3 plasma can reduce current collapse and increase reliability for microwave operation of SiN_x/AlGaN/GaN HEMTs. The improved performance is possibly associated with incorporated H^+, which may passivate bulk defects in GaN.

There has also been success with postmetallization treatments. For example, Peng *et al.*[302] demonstrated that postmetallization annealing (PMA) at 350 °C in N_2 on SiN_x/AlGaN/GaN HEMTs improves the direct-current, radio-frequency small signal, and power performance. It is suggested that PMA improves the quality of the passivation layer by N diffusion through the SiN_x into N vacancies in the AlGaN, suppressing current collapse; the plasma process may also recover the dry-etch damage at the Schottky metal/AlGaN interface, reducing leakage current. Similarly, Zhou *et al.*[303] found improved DC performance of ALD Al_2O_3/AlGaN/GaN HEMTs after 10 min 600 °C PDA in N_2 atmosphere. This treatment reduces deep-level traps, ultimately increasing the maximum transconductance and gate-drain breakdown voltage. Other studies by Wu *et al.*[114] reported the D_{it} of ALD-Al_2O_3/GaN MOS structures is reduced from $\sim 1.5 \times 10^{12}$ $cm^{-2}\,eV^{-1}$ to 7×10^{10} $cm^{-2}\,eV^{-1}$ after 800 °C PMA in N_2, and Lin *et al.*[306] reported on the reduction in the leakage current in AlGaN/GaN HEMTs by three orders of magnitude by PMA in N_2/H_2.

In other words, it is clear that postdeposition or postmetallization treatment plays a role in improving passivation effects and reducing current collapse and gate leakage. Most studies agree that PDA in some form of N_2 plasma or PMA in some form of N_2 gas ambient are effective ways at increasing device performance; however, it is not clear how the treatment passivates culpable electronic states.

V. SUMMARY AND CONCLUSIONS

In summary, while research has addressed the properties and impact of electronic states, there is still a need for concentrated efforts to provide a more comprehensive understanding of interface and surface electronic states. It is clear from gate leakage and current collapse measurements that improving surface state passivation will play an integral part in mitigating failure mechanisms and augmenting device reliability. From polarization and band bending, we can determine that there is a significant density of states (10^{13} states/cm^2) at the surface of GaN and AlN. *Ab initio* calculations seemingly imply that these surface states are associated with vacancies and vacancy complexes; however, such a pristine surface is rarely achieved on GaN or AlN, which are typically contaminated with high concentrations of structural defects, point defects, surface contamination, and native oxide. Cleaning and surface processing is therefore an important step in device fabrication, where several cleans have been proven to increase device performance. For example, NH_4OH relative to acid etches was shown to improve device performance because of decreased Ga_2O_3 coverage. These results would suggest that the native oxide may be more influential than carbon, since the carbon contamination is often larger on NH_4OH cleaned samples. On the other hand, other research has shown that carbon is detrimental to device performance. Given the intricacy of the states, it is difficult to compare the impact of specific cleaning processes. Other cleaning processes were more successful at removing both oxygen and carbon contaminations, but they may have been at the expense of increasing other defects such as Ga or N vacancies. In some other cases, cleaning even produced stoichiometric GaN with contamination levels below the sensitivity of surface analysis techniques. However, such samples have not been connected with any specific surface

reconstruction or device behavior. It thus remains unclear whether these samples have effectively mitigated the effects of the surface states. Furthermore, device structure requires the deposition of a passivation scheme, gate dielectric, and/or ohmic contact on the surface, which induces interface gap states as well as additional defect damage depending on the deposition process. There have been studies to evaluate the induced interface defects. While it is difficult to compare these studies given the multitudes of variables, research suggests Al_2O_3 and N_2 plasma currently show the most promise, producing surfaces with an interface trap density on the order of 10^{-10} charges/cm^2. In other words, of the $\sim 10^{13}$ states/cm^2 required to screen the polarization bound charge, approximately one in every 1000 serves as an electron trap. This is a significant improvement. However, given the complexity and subtlety of the electronic state configuration, a more systematic and comprehensive approach may be needed to fully optimize device performance.

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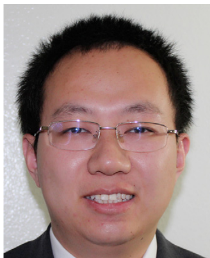

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