

# Enhanced tunneling in stacked gate dielectrics with ultra-thin $\text{HfO}_2$ layers sandwiched between thicker $\text{SiO}_2$ layers

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## Abstract

There has been a search for alternative dielectrics with significantly increased dielectric constants,  $K$ , which increases physical thickness in proportion to  $K$ , and therefore would significantly reduce direct tunneling. However, *increases* in  $K$  to values of 15–25 in transition metal and rare earth oxides are generally accompanied by *decreases* in the conduction band offset energy with respect to Si,  $E_B$ , and the effective electron tunneling mass,  $m_{\text{eff}}$ , which mitigate gains from increased thickness. A novel technique, based on stacked dielectrics, is used to obtain the tunneling mass-conduction band offset energy product. When combined with optical measurements of tunneling barriers, this yields direct estimates of the tunneling mass.

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**Keywords:** High- $K$  dielectrics; Direct tunneling; Tunneling mass-conduction band offset energy product; Stacked gate dielectrics

## 1. Introduction

In order to reduce direct tunneling in metal oxide semiconductor, MOS, devices with equivalent oxide thickness, EOT, less than 1.5 nm, and extending below 1 nm, there has been a search for alternative dielectrics with significantly increased dielectric constants,  $K$ , allowing increases in physical thickness proportional to  $K$ , and thereby having the potential to significantly reduce direct tunneling. However, large *increases* in  $K$  to values of 15–25 in transition metal and rare earth oxides are generally accompanied by decreases in the conduction band offset energy with respect to Si,  $E_B$ , and the effective electron tunneling mass,  $m_{\text{eff}}$ . Direct tunneling scales as an exponential function of the dielectric constant,  $K$ , times the square root of the

$(E_{\text{Bi}})(m_{\text{eff}})$  product. It is therefore important to determine this product in order to estimate the extent to which decreases in the product can mitigate decreases in tunneling anticipated from increases physical thickness which are proportional to  $K$ . This paper presents a novel method for obtaining the  $(E_{\text{Bi}})(m_{\text{eff}})$  product for high- $K$  gate dielectrics. It is based on a quantum mechanical *WKB approximation* applied to large bias dependent *increases* in tunneling in *symmetric stacked devices* with ultra-thin  $\text{HfO}_2$  layers (–0.5 nm) sandwiched between thicker  $\text{SiO}_2$  layers (–1.0 to 1.5 nm). Tunneling currents in these devices are compared to reference  $\text{SiO}_2$  devices and values for the  $(E_{\text{Bi}})(m_{\text{eff}})$  product are obtained. The extension to other high- $K$  alternative dielectrics is straightforward and obvious.

In addition to providing a method for obtaining the  $(E_{\text{Bi}})(m_{\text{eff}})$  product, the results presented below are of importance for advanced dielectrics with stacked high- $K$  components with different dielectric constants,  $K$ , tunneling barriers,  $E_B$ , and effective tunneling

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masses,  $m_{\text{eff}}$ , for example, in MOS devices with laminated  $\text{HfO}_2\text{--Al}_2\text{O}_3$  dielectrics as in [1,2].

## 2. Experimental results

Stacked structures were prepared with remote plasma processed Si– $\text{SiO}_2$  substrates 1.5 nm thick, remote plasma deposited  $\text{HfO}_2$  layers 0.5–5.0 nm thick, and  $\text{SiO}_2$  layers 1.5 nm thick [3].  $N^+$  Si substrates and Al metal gates were used to set the flat band voltage,  $V_{\text{fb}}$ , of the stacked structures close to zero. Analyses of capacitance–voltage,  $C\text{--}V$ , traces were based on the profile in Fig. 1.

The increased thickness of  $\sim 1.2$  nm in Fig. 1 for an initially-deposited and *encapsulated* 0.5 nm  $\text{HfO}_2$  film is due to interfacial Hf *silicate formation* during deposition and annealing as has been identified by on-line X-ray photoelectron spectroscopy, XPS. There is also an accompanying reduction of the  $\text{SiO}_2$  layer thicknesses from 1.5 to 1.2 nm. Values of EOT were determined from  $C\text{--}V$  measurements using the procedures developed by Hauser [4]. EOT decreased from  $\sim 2.97$  nm for the  $\text{SiO}_2$  reference device with 3 nm of  $\text{SiO}_2$ , to  $\sim 2.75$  nm for the  $\text{HfO}_2$  device with the initially-deposited 0.5 nm  $\text{HfO}_2$  layer. The analysis of the  $C\text{--}V$  data based on Fig. 1 gives a value of  $K$  of  $\sim 20$  for the middle layer consistent with a silicate

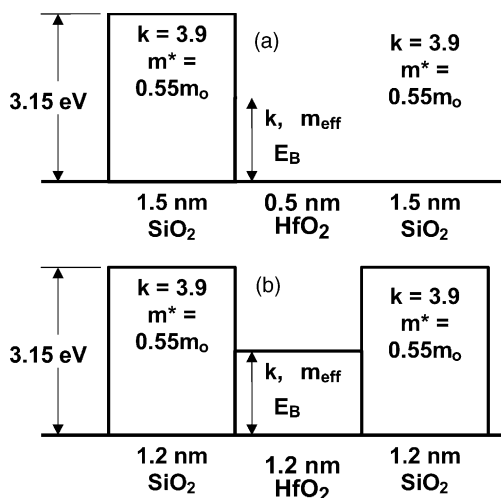


Fig. 1. Barrier layer model for the stacked dielectrics in Fig. 2 with 0.5 nm as-deposited  $\text{HfO}_2$ : (a) as-deposited; (b) after device processing, including 900 °C.

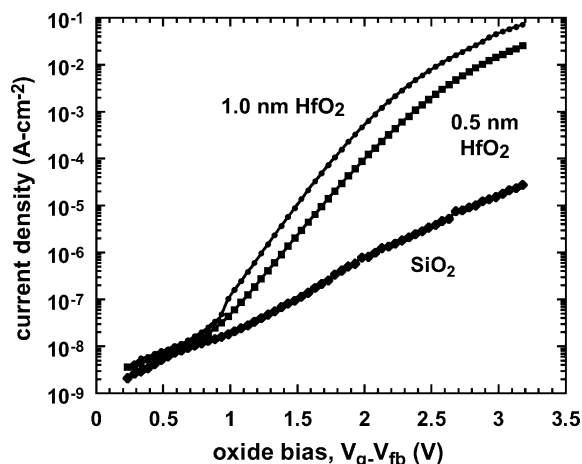


Fig. 2. Room temperature  $J\text{--}V$  characteristics for 3 nm  $\text{SiO}_2$  and two stacked devices with 0.5 and 1.0 nm of as-deposited  $\text{HfO}_2$ . The dashed line and arrow define the voltage regime in which the tunneling current is not limited by the sensitivity of the measurement defined by the magnitude of the displacement current.

terminated  $\text{HfO}_2$  structure. Current density versus voltage,  $J\text{--}V$  traces were obtained in a substrate injection mode. Fig. 2 compares room temperature  $J\text{--}V$  traces for a MOS capacitor, MOSCAP, with a 3.0 nm  $\text{SiO}_2$  dielectric, with traces for MOSCAP stacks including *initially-deposited* 0.5 and 1.0 nm  $\text{HfO}_2$  films. The  $J\text{--}V$  characteristic for the  $\text{SiO}_2$  reference device is in agreement with a  $J\text{--}V$  simulation of [5]. All  $J\text{--}V$  curves display a similar weak temperature dependence confirming that tunneling is the dominant transport mechanism.  $J\text{--}V$  curves for the stacked devices are qualitatively different than the  $\text{SiO}_2$  device, displaying bias voltage dependent increases in current at 3 V of  $\sim 1000$  for the 0.5 nm  $\text{HfO}_2$  device and  $\sim 3000$  for 1.0  $\text{HfO}_2$  device. These devices have an area of  $\sim 10^{-4} \text{ cm}^2$ . Since the displacement current, determined the voltage ramp rate was  $\sim 10^{-12} \text{ A}$  (or equivalently  $10^{-8} \text{ A/cm}^2$ ), the  $J\text{--}V$  plots are valid for voltages greater than about 1.2 V.

## 3. Analysis of tunneling data in devices with stacked dielectrics

The objective of this section is to provide an explanation for the significant increases in tunneling

current in the stacked-dielectric MOSCAPs of Fig. 2. These increases reflect changes in the energy of the tunneling electron relative to the dielectric conduction band as it *traverses* the dielectric, and for a homogeneous SiO<sub>2</sub> dielectric and the stacked dielectric of Fig. 1.

The departure from a near exponential dependence in the reference SiO<sub>2</sub> device is correlated with differences between the tunneling attenuation constants,  $\alpha_i t_i$  in the three regions of the stacked dielectric of Fig. 3(a). If  $E_{Bi}$  is the tunneling barrier with respect

to the substrate/gate metal Fermi level, and  $m_{\text{eff}i}$  is tunneling mass, then the tunneling attenuation factor for the  $i^{\text{th}}$  layer,  $\alpha_i t_i$ , is given by  $4\pi t_i (2m_{\text{eff}i} E_{Bi})^{0.5} / h$  with  $i = 1, 2$ , and 3 for the stacked device, and  $i = 1$  for the homogeneous SiO<sub>2</sub> device. Neglecting reflections at potential steps in Fig. 1 for the device with the composite, or stacked dielectric, the relative tunneling current is proportional to the product of the transmission layer attenuation constants,  $\prod_i \exp(-\alpha_i t_i)$  [5]. This WKB approach is supported by plots in Fig. 3(a) and (b). The data in Fig. 3(b) have been fit by setting  $(E_{Bi})(m_{\text{eff}}) = 0.23 \pm 0.01 m_0$  for HfO<sub>2</sub>. This value was obtained by iterating between the plots in Fig. 3(a) and (b) until an acceptable fit between the calculation and experiment was obtained. Using a nominal value of  $E_B \sim 1.5$  eV for the Si–HfO<sub>2</sub> conduction band offset energy, this corresponds to a value of  $m_{\text{eff}} = 0.15 \pm 0.02 m_0$ , in good agreement with other analyses of tunneling through HfO<sub>2</sub> films [6].

The values of  $\alpha_i t_i^*$  as a function of bias in Fig. 3(a) are obtained by assuming the applied potential drops in the three regions of Fig. 1 are proportional to the relative values of  $K$ , i.e. the continuity of  $K_i \epsilon_0 E_i$ , where  $E_i$  is the electric field in the  $i^{\text{th}}$  region. The sum of  $E_i t_i$ 's is set equal to the bias voltage across the oxide,  $V_g - V_{fb}$ . After the iterations, the product of the  $\alpha_i t_i^*$ 's is eventually used for the fit in Fig. 3(b), so that values of  $E_{Bi}$  can be obtained and inserted in the  $\alpha_i t_i^*$  for HfO<sub>2</sub>.  $E_{Bi}(V)$  values are approximated by  $E_{Bi}(0)$  minus the average potential drop in that region, with  $t_i^*$  normalized to 1.2 nm. The relatively small decreases in  $\alpha(\text{SiO}_2)$  compared to larger decreases in  $\alpha(\text{HfO}_2)$  are due the differences in the  $E_{Bi}(0)$ , 3.15 eV for SiO<sub>2</sub> and 1.5 eV for HfO<sub>2</sub>, and are reflected in the marked increase in their ratio with increasing bias. This means that as the bias across the composite in these films is increased, the current is increasingly determined by the SiO<sub>2</sub> layers. The increased ratio of current at 3 V is  $\sim 1000$  is due to *minimal wave function attenuation* in the HfO<sub>2</sub> layer. This decreases the SiO<sub>2</sub> thickness from 3.0 in the reference device to an *effective thickness* of 2.4 nm in the stacked device; i.e. a  $10\times$  increase in current for each 0.2 nm thickness decrease. This explanation is supported in Fig. 3(b), which displays ratios of measured currents, and normalized transmission for the SiO<sub>2</sub> stack component, both as functions of the ratio of the normalized attenuation constants. The experimental  $J$ – $V$  characteristics are valid for

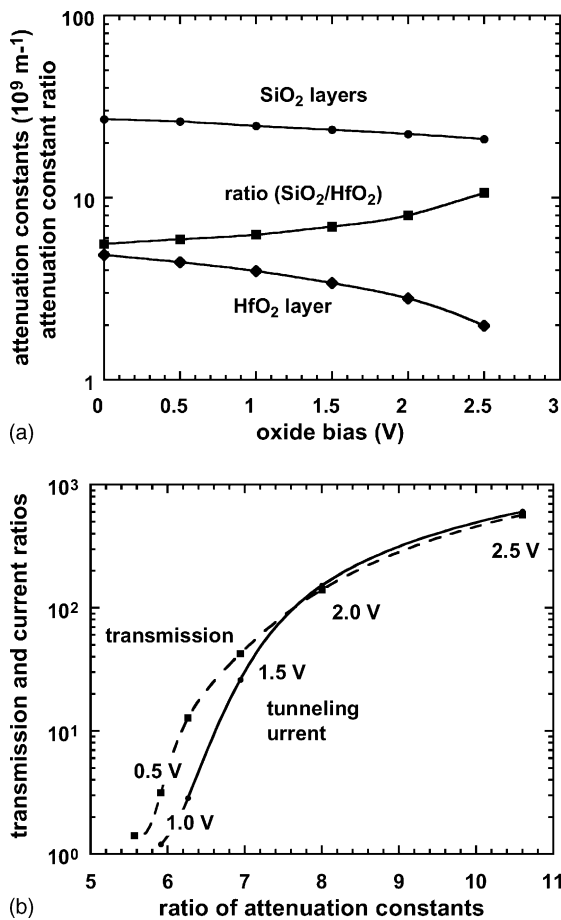


Fig. 3. (a) Transmission attenuation constants for SiO<sub>2</sub> and HfO<sub>2</sub> layers, and their ratio vs. oxide bias. (b) Current ratio, and normalized transmission ratio vs. ratio of SiO<sub>2</sub>/HfO<sub>2</sub> attenuation constants of Fig. 3(a). Bias voltages are indicated as well. The dashed line and arrow define the voltage regime in which the tunneling current is not limited by the sensitivity of the measurement as defined by the magnitude of the displacement current.

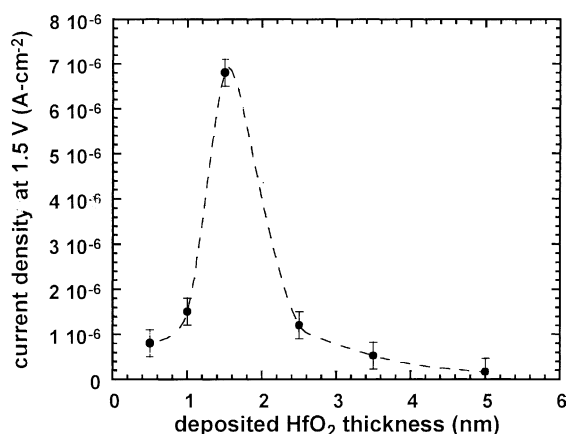


Fig. 4. Current density at 1.5 oxide bias as a function of deposited HfO<sub>2</sub> layer thickness.

current densities greater than about  $5 \times 10^{-8} \text{ A/cm}^2$ , and hence the experimental results and attenuation constant model calculations should be compared for bias voltages  $>1.1\text{--}1.2 \text{ V}$ , and attenuation constant ratios greater than about 6.7.

If the thickness of the HfO<sub>2</sub> layer is *increased* by  $>5$ , instead of current increasing with increasing bias, it is reduced relative to the SiO<sub>2</sub> device. Identifying the HfO<sub>2</sub> thickness at which this change occurs yields a direct measure for an approximate high- $K$  dielectric  $(m_{\text{eff}})(E_{\text{Bi}})$  product.

Fig. 4 is a plot of the current density at an oxide bias of 1.5 V as function of the thickness of the as-deposited HfO<sub>2</sub> layer. The shape of the  $J$ – $V$  characteristic, along with this plot suggests that a resonant tunneling mechanism may be the origin of the enhanced current flow in the HfO<sub>2</sub> thickness regime centered at about 1.5 nm.

#### 4. Discussion and conclusions

This paper has demonstrated a new approach for obtaining the  $(m_{\text{eff}})(E_{\text{Bi}})$  product for high- $K$  dielectrics. In addition, the results presented above identify a significant limitation for stacked dielectrics in which the band offset energy and dielectric constant of one component are significantly less than in the second, as for example in HfO<sub>2</sub>–Al<sub>2</sub>O<sub>3</sub> laminates, where  $m_{\text{eff}} \sim 0.15m_0$  and  $E_{\text{B}} = 1.5 \text{ eV}$ , and Al<sub>2</sub>O<sub>3</sub>, where  $m_{\text{eff}} \sim 0.4m_0$  and  $E_{\text{B}} = 2.7 \text{ eV}$ , and where the

respective  $K$ -values are  $\sim 20\text{--}25$  for HfO<sub>2</sub> and  $\sim 9$  for Al<sub>2</sub>O<sub>3</sub>. The  $J$ – $V$  tunneling curve will display a significant rise in current for bias voltages greater than 1 eV, which may be detrimental in mobile device applications.

Next, it is important to comment on the magnitude of the low effective value for tunneling mass for HfO<sub>2</sub>, and its impact on direct tunneling in silicate alloys. It is significantly smaller than the mass of  $\sim 0.55m_0$  for SiO<sub>2</sub> and it is important to understand the microscopic origin for this difference. Fig. 5 contains a plot of tunneling mass versus band offset energy that is consistent with the Franz two-band model of [7,8]. The masses for vacuum, SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> and Si<sub>3</sub>N<sub>4</sub> dielectrics fall on a straight line, along with the extrapolated mass for Y<sub>2</sub>O<sub>3</sub>; however the mass for HfO<sub>2</sub> does not. The Franz two-band model is an effective mass approximation that works best when the conduction and valence band states are extended and free electron like. This is the case for SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>, where the lowest conduction band states are 3s\* anti-bonding states, and it is a good approximation for Si<sub>3</sub>N<sub>4</sub> where the Si 3s\* state dominates. The lowest conduction band states in transition metal oxides are anti-bond transition metal d\* states; however the overlap of these states with transition metal s\* states differs and is proportional to the difference between the

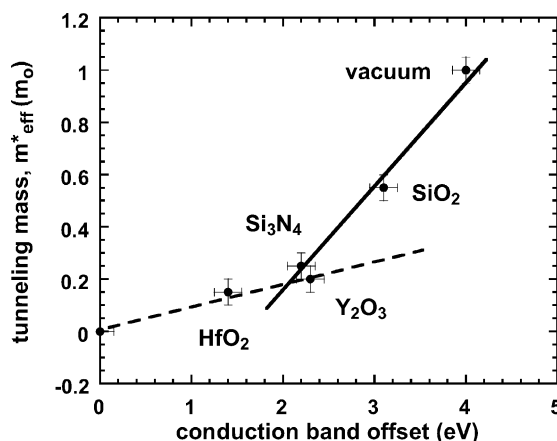


Fig. 5. Plot of the tunneling mass vs. the conduction band offset energy with respect to silicon. The solid line is what is expected on the basis of the Franz two-band model for conduction band states that are extended in character. The dotted line represents the changes that occur when the conduction band states are localized as in the transition metal and rare dielectrics.

atomic  $nd$  and  $n+1s$  states of the transition metal;  $n$  is the principal quantum number equal to 5 for Hf and 4 for Y. The point for  $Y_2O_3$  falls on the plot for the oxides with extended free electron like conduction band states, and the point for  $HfO_2$  is well removed from this fit to the data due primarily to differences in  $s$ – $d$  overlap which is greater the  $Y_2O_3$ . Finally, it has been shown in [9] that the low value of  $m_{eff} = 0.15m_0$  coupled with an  $E_B \sim 1.5$  eV gives a minimum tunneling current for a given EOT in the middle of the silicate alloy regime, whereas for Y silicates, the higher values of both  $m_{eff} \sim 0.25m_0$  and  $E_B \sim 2.3$  gives a minimum tunneling current very close to the  $Y_2O_3$  composition as displayed in Fig. 6. Fig. 6 presents the compositional dependence of tunneling current density at an oxide bias of 1 V as calculated using the WKB approximation. The plots in Fig. 7 are for the figure of merit,  $\Phi_m$ , for direct tunneling as is given by:

$$\Phi_m = K[E_B m_{eff}]^{0.5} \quad (1)$$

where  $K$ ,  $E_B$  and  $m_{eff}^*$  have been computed for Si oxynitride alloys, Hf silicate alloys and Zr silicate alloys using compositionally averaged values of  $K$ ,  $E_B$  and  $m_{eff}$ . The plots in Fig. 6 are for the direct tunneling current in  $n$ +-dielectric- $N$ +-poly-Si at an oxide bias of in excess of 1 V above flat band for substrate

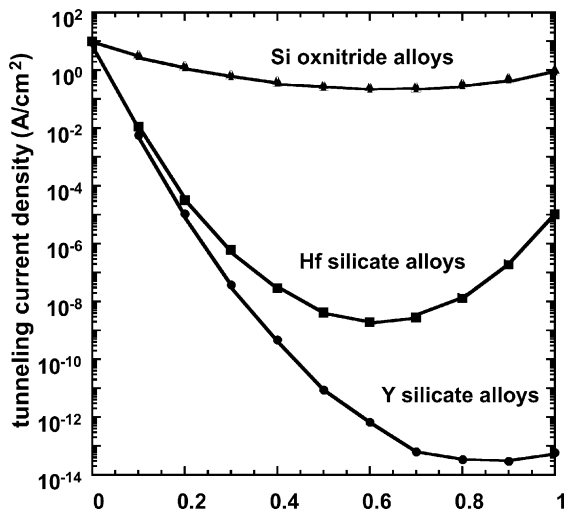


Fig. 6. Calculated direct tunneling currents for an oxide bias of 1 V, and for an equivalent oxide thickness of 1.2 nm for Si oxynitride alloys, Hf silicate alloys and Y silicate alloys as function of alloy composition as based on a WKB model calculation.

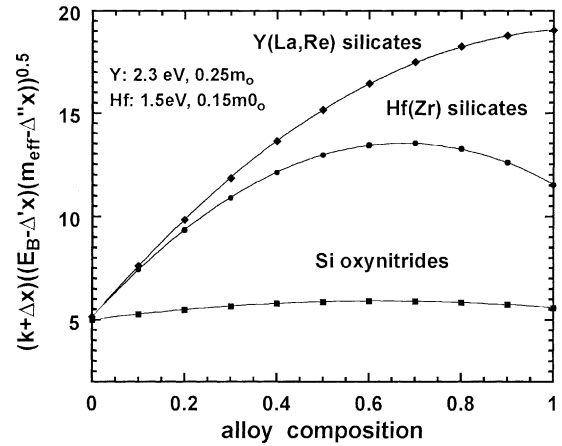


Fig. 7. Plots of the tunneling figure of merit for Si oxynitride alloys ( $E_B = 3.13$ – $5$  eV for  $SiO_2$ , and  $2.15$  eV for  $Si_3N_4$ ,  $m_{eff} = 0.55m_0$  for  $SiO_2$  and  $0.25m_0$  for  $Si_3N_4$ , and  $K = 3.8$  for  $SiO_2$  and  $7.6$  for  $Si_3N_4$ ), Hf silicates ( $E_B = 1.5$  eV,  $m_{eff} = 0.15m_0$  and  $K = 25$  for  $HfO_2$ ) and Y silicates ( $E_B = 1.5$  eV,  $m_{eff} = 0.25m_0$  and  $K = 25$  for  $Y_2O_3$ ). The calculations use compositionally averaged values of  $E_B$ ,  $m_{eff}$  and  $K$ .

accumulation. The calculation takes into account the potential drops across the poly-Si and the channel region, so that there is a potential drop of 1 V across the dielectric for the gate potential used in the evaluation of the current density [9]. The doping concentration in the substrate was  $2.5 \times 10^{17} \text{ cm}^{-3}$ , and in the poly-Si,  $9 \times 10^{19} \text{ cm}^{-3}$ . The values of the computed tunneling current density are independent of these values for  $n$ +- and  $N$ +- because of the corrections made for the potential drops in the poly-Si and channel regions of the dielectric stack. The differences between the calculated compositional variations of direct tunneling in Hf and Y silicate alloys represent the importance for determining the  $(E_B)(m_{eff})$  product for high- $K$  dielectrics, which can be accomplished through the novel approach identified in this article. The correlation between the tunneling figures of merit in Fig. 7 and the calculated tunneling currents in Fig. 6 is evident in the complementary nature of the plots.

Finally, experiments have verified the dependence of tunneling current on alloy composition for Hf silicate alloys [9]. This has important implications for advanced devices. The decrease of tunneling current for alloys compositions between 30 and 60%  $HfO_2$  in silicate alloys relative to the end-member  $HfO_2$  is accompanied by a significant decrease in the

dielectric constant, from  $\sim 20$  to 25 in  $\text{HfO}_2$  to between 10 and 15 in the lower  $\text{HfO}_2$  content silicate alloys. This has a significant effect on the attainable values of EOT, particularly when thin  $\text{SiO}_2$  interfacial layers are taken into account. These issues are currently being addressed with respect to optimized devices for high performance and mobile devices.

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