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Diamond Schottky p-i-n diodes for high power RF receiver protectors

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ABSTRACT

The electrical characteristics of diamond Schottky p-i-n diodes grown by plasma enhanced chemical vapor deposition have been measured from DC to 25 GHz and used to extract the small-signal parameters for a lumped-element compact model. The model accurately reproduces the forward and reverse bias DC characteristics, the capacitance-voltage behavior, as well as the insertion and reflection loss. The high thermal conductivity of diamond makes the diodes ideally suited for high power radar receiver protector applications. We demonstrate that under forward bias a single diode can provide 14 dB of input power attenuation. For self-biased limiter applications, a two-stage circuit with back-to-back diodes has been simulated using the diode model to show > 20 dB of attenuation at an input power of 50 dBm.

1. Introduction

Progress in the growth of boron [1–4] and phosphorus doped [5–9] diamond thin films has led to the demonstration of ultra-wide band gap semiconductor junction diodes [10–12], field effect transistors [13–20], and bipolar junction transistors [21,22]. P-type diamond Schottky diodes with off-state blocking voltages of 10 kV have been demonstrated [23], as well as room temperature current densities of >60 kA/cm^2 at a forward bias of 6 V [24]. The high thermal conductivity of diamond, combined with a high breakdown field and the ability to support large current densities, suggest that these devices will find practical application in systems that require high power density. Indeed, progress towards high power DC-DC switching converters suggests that diamond-based solutions will compare favorably to other wide band gap materials such as SiC and GaN [25].

Alongside the progress being made towards diamond electronics for DC power management, diamond devices are also being developed for high power RF applications. The two-dimensional hole gas (2DHG) formed at the surface of hydrogen terminated diamond has been used for p-channel FETs with a cutoff frequency, f_T, and maximum oscillation frequency, f_{max}, of 41 GHz and 44 GHz respectively [26]. The 2DHG p-FETs are also capable of high current drive with drain currents in excess of 1 A/mm [27]. Diamond MOSFET RF amplifiers with 3.8 W/mm of output power at 1 GHz have been demonstrated [28]. These results bode well for RF power amplifiers that would benefit from the efficient heat-sinking enabled by the high thermal conductivity of the diamond substrate.

Receiver protectors are another application that would benefit from the superior power handling capability of diamond electronics. Diode receiver protectors can be operated as active attenuators [29] in which an external bias is used to switch the diode from a low insertion loss, off-state, to a highly attenuating conducting state, for which the input power is reflected. Alternatively, back-to-back diodes can be used as self-biased passive attenuators that turn on when high RF powers are present at the input of sensitive receiver elements. Commercial silicon p-i-n diode limiters are widely available for receiver protector applications [30]. Integrated GaAs p-i-n passive limiters have been demonstrated for CW input powers of 4 W [31]. Achieving receiver protection for input RF powers in the range 10–100 W is a challenge for existing semiconductor technologies, in part because of the difficulty in extracting the heat from the diodes caused by the absorbed power not reflected by the impedance mismatch. Diamond, with the highest thermal conductivity of any known material, may offer a solution for high power receiver protector applications.

In previous work [32] we have demonstrated a Schottky p-i-n diode active receiver protector capable of 14 dB of input power attenuation under strong forward bias conditions. In this paper we extend the work as follows. Section 2 summarizes the thin film diamond growth while

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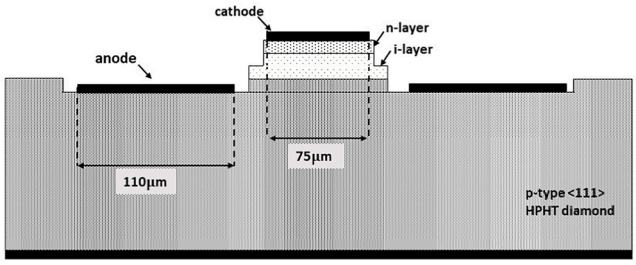

Fig. 1. Schematic cross-section of the diamond Schottky p-i-n diode. The devices are electrically isolated by a partial etch that finishes within the high resistance i-layer. A second, deeper etch is used to make contact to the p-type substrate from the top surface.

Section 3 details the fabrication of the Schottky p-i-n diodes. Section 4 describes the DC and AC measurements of the current–voltage and capacitance–voltage characteristics used to extract the small-signal parameters for the lumped-element compact model development in Section 5. The model is then calibrated against measured data of the 2-port S-parameters in Section 6, and used to simulate a two-stage, passive receiver protector circuit in Section 7. We finish with concluding comments in Section 8.

2. Diamond layer growth

A schematic cross-section of the diamond Schottky diodes used for the compact model parameter extraction is shown in Fig. 1. Growth of the diamond layers was performed by plasma enhanced chemical vapor deposition (PECVD) onto high-pressure, high-temperature (HPHT) monocrystal type IIb diamond plates [33], laser cut and polished to a size of $3 \times 3 \times 0.3$ mm (tolerance $\pm$ 0.05 mm). The HPHT substrates had a crystallographic orientation of (1 1 1) and an off-angle minimal miscut of $\pm$ 1.5 deg. The roughness of the polished surfaces prior to epi-layer growth was $\sim$ 40 nm. Secondary ion mass spectroscopy (SIMS) characterization confirmed a boron concentration of $> 1.9 \times 10^{20}$ cm^{-3}.

The substrate was prepared for epi-layer growth by a wet-chemical cleaning process that commenced with boiling in an acid mixture (H_2SO_4 /H_2O_2 /H_2O, 3:1:1) at 220 °C for 15 min to remove organic and metallic contamination. This was followed by HF treatment for 5 min to remove oxide layers. The final step included a boil in (NH_4OH/H_2O_2 /H_2O, 1:1:5) at 75 °C for 15 min to remove the surface adhered particles and organic contamination. After each step the substrate was rinsed with deionized water.

After cleaning, the substrate was loaded into an ASTeX® style intrinsic diamond growth PECVD reactor with a base pressure in the mid 10^{-8} Torr. Prior to growth the substrate surface was exposed to a pure hydrogen plasma (H_2 flow rate 400 sccm, microwave power 950 W, chamber pressure 55 Torr) at around 730 °C for 5 min. Intrinsic diamond growth commenced by establishing a methane flow rate of 6 sccm and oxygen flow rate of 0.75 sccm with the hydrogen flow rate adjusted to maintain a total gas flow rate of 400 sccm. The microwave power was set to 1000 W and the chamber pressure to 55 Torr, resulting in a growth temperature of about 800 °C. Growth was terminated after 110 min to target an intrinsic diamond layer thickness of 300 nm. The sample was then transferred to another PECVD system dedicated to phosphorus doped diamond growth and with a similar ASTeX® style configuration. An initial exposure of the intrinsic diamond layer to a pure hydrogen plasma (H_2 flow rate 400 sccm, microwave power 1300 W, chamber pressure 60 Torr) at about 700 °C for 5 min prepared the surface for phosphorus doped diamond homoepitaxy. With a methane flow rate of 0.5 sccm, a 200 ppm trimethlyphosphine in hydrogen mixture presented the dopant source with a flow rate of 40 sccm. A hydrogen flow was established for a total gas flow rate of 400 sccm. With a microwave power of 2000 W and a chamber pressure of 60 Torr the growth temperature was recorded by a dual-wavelength pyrometer and measured to be 850 °C. Growth of the phosphorus doped diamond layer was terminated after 7 min resulting in a highly doped n-type layer of thickness $\sim$ 50 nm.

To determine the doping concentrations in the diamond epi-layers, test layers were grown to calibrate the phosphorus concentration in the n-layer and the background doping in the intrinsic layer using SIMS profiling. For the intrinsic diamond layer a nitrogen concentration $< 5 \times 10^{17}$ cm^{-3} and a boron concentration $< 7 \times 10^{15}$cm^{-3} are typically measured. For n-type layers grown under similar conditions a peak phosphorus concentration of $>10^{19}$ cm^{-3} are routinely achieved. While the doping concentrations in the sample used for the p-i-n diode described here were not measured directly with SIMS, our experience confirms that similar growth conditions result in similar impurity incorporations.

Table 1
RIE conditions used to etch the diamond diodes.

	Gas Chemistry and Flow Rate (sccm)		Pressure (mTorr)	Power (W)	Etch Rate (nm/min)
Diamond Etch	SF_6	O_2	15	300	24
	2	38			
SiO_2 Etch	Ar	CHF_3	30	200	46
	25	25			

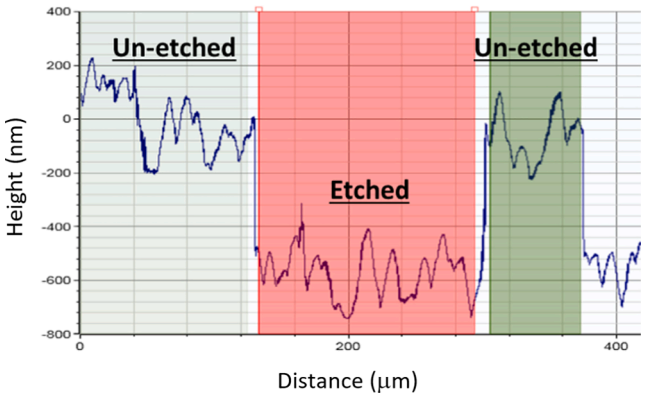

Fig. 2. Height profile of diamond sample post diamond etching and after removal of the SiO_2 hard mask.

3. Diode fabrication

The diodes were fabricated with electrical contacts suitable for on-wafer DC and RF probing as follows. To electrically isolate the devices from one another, a 2-step reactive ion etch (RIE) process was used to define a mesa structure. The first step involved the blanket deposition of a 1 µm thick SiO_2 layer that was patterned by photolithography and then etched using an Ar/CHF_3 gas mixture. The patterned SiO_2 then serves as a hard mask for the second RIE step, during which an SF_6/O_2 gas mixture is used to etch the diamond, through the n-type surface layer into the high resistance i-layer. To allow contact to the p-type region from the top surface, RIE was again used to etch through the i-layer and into the HPHT substrate, once more using a 2-step process with an oxide hard mask. The RIE etch conditions are summarized in Table 1 and have been optimized to minimize in-situ sputtering and micromasking. A profilometry measurement was done after diamond etching using a Bruker Dektak XT profilometer and after stripping off the residual SiO_2 hard mask. Fig. 2 shows a profile of the diamond surface post etching. The etch depth is approximately 600 nm as measured between two mesa

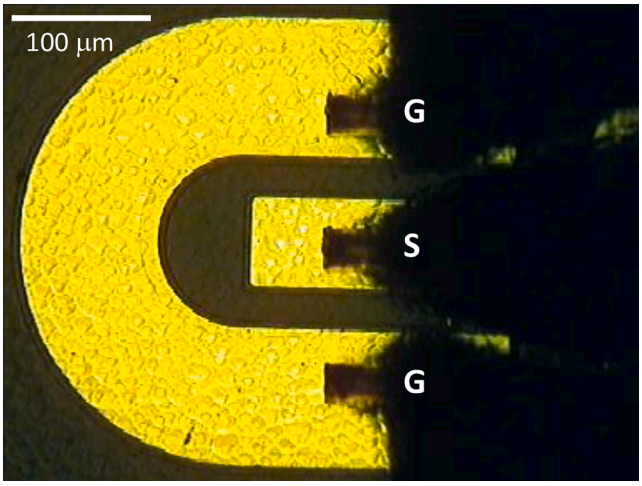

Fig. 3. Optical micrograph showing the top surface of the diamond diode with a ground-signal-ground (GSG) RF probe placed onto the device. The active area of the diode beneath the central anode contact is 110 μm × 75 μm.

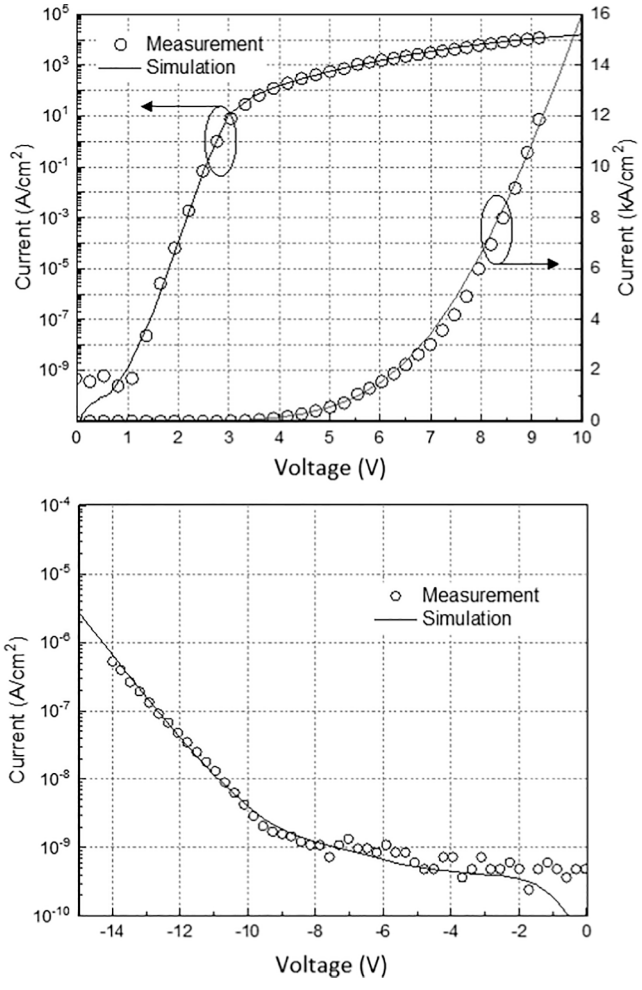

Fig. 4. The measured forward (top) and reverse bias (bottom) DC IV characteristics. The data is recorded every 20 mV but only a subset is included in the plot so as not to obscure the fit to the data (solid line) for the compact model sub-circuit of Fig. 8. The noise floor of the measurement instrument is ~ 50 fA corresponding to a current density of ~ 7×10^{-10} A/cm^2.

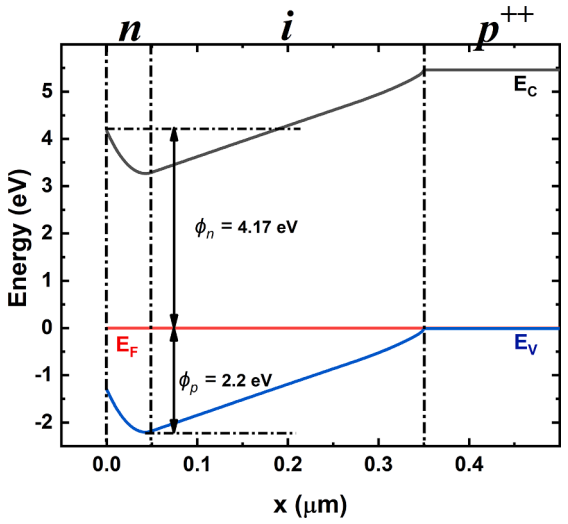

Fig. 5. Energy band diagram of the diamond p-i-n diodes at 0 V bias, derived from a numerical model using the parameters in Table 2. The band bending at the surface of the device confirms that the n-type layer is full depleted.

structures separated by an etched region of width 160 μm. Comparing the unetched to the etched regions of the diamond in Fig. 2, the sample roughness has remained the same at approximately 150 nm. This confirms that reactive ion etching of the diamond layers does not introduce any significant roughness beyond that present after the epitaxial growth. However, the surface roughness is greater than the ~ 40 nm of the polished HPHT substrates before the epitaxial layers are grown. The boron-doped, HPHT diamond maintains single crystal character through boron concentration of ~ 2×10^{20} cm^{-3} [33], and we suggest that the additional roughness is likely related to vicinal surface facets that form during the homoepitaxial growth.

Metal layers of Ti/Ni/Au (50 nm/50 nm/300 nm) were deposited by electron beam evaporation to form the cathode and anode contacts to the n- and p-layer diamond respectively. The contacts were not annealed, but the metal layer to the anode forms a tunneling Ohmic contact due to the high doping concentration in the p-type diamond substrate. In contrast, a Schottky contact is formed on the less heavily doped n-type cathode. The electrical contacts were patterned with a ground-signal-ground (GSG) configuration as shown in Fig. 3. The active diode area of 100 μm × 75 μm forms the central signal connection, and the center-center pitch between the ground-signal pads is 100 μm. The texture that is apparent in the metal contacts is due to the surface roughness present on the diamond epilayers as discussed above.

4. DC and AC characterization

The electrical characteristics of the diodes were measured by on-wafer probing. The DC IV data characteristics are shown in Fig. 4. For reverse bias and forward bias up to 6 V, the current was measured using an Agilent 4156 precision semiconductor parameter analyzer with a maximum current of 100 mA and a noise floor of 50 fA. For higher currents the forward IV characteristics were recorded using a Keithley 2400 with a current limit of 1A. The current limit was reached at a forward bias of 9.2 V and corresponds to a current density of 12.1 kA/cm^2. The solid line is the fit to the measured data using the lumped element diode model described in Section 5.

As mentioned in Section 3, the devices used for this work are considered to be Schottky p-i-n diodes because the n-type layer is fully depleted by the Schottky barrier formed by the anode contact [34]. One indication of Schottky p-i-n behavior is a lower turn-on voltage compared to p-i-n diodes with thicker, undepleted n-layers. For example, the diode current in Fig. 4 starts to increase exponentially at a

Table 2
Summary table of the parameters used for the TCAD numerical simulations of Fig. 5 [36].

	Parameter	Value	Units
Cathode contact	Metal work function, ϕ_m	4.5	eV
Diamond n-layer (heavy doping)	Donor concentration, N_D	3×810^{17}	cm^{-3}
	Donor activation energy, E_D	0.57	eV
Diamond i-layer (background doping)	Acceptor concentration, N_A	4×10^{14}	cm^{-3}
	Acceptor activation energy, E_A	0.51	eV
Diamond p-layer (heavy doping)	Acceptor concentration, N_A'	3×10^{20}	cm^{-3}
	Acceptor activation energy, E_A'	0.052	eV
Anode contact	Ohmic	N/A	N/A

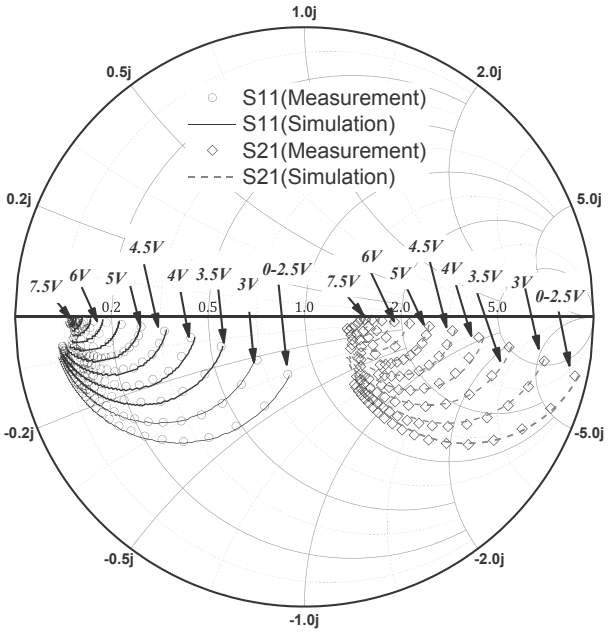

Fig. 6. The measured S_{11} (circles) and S_{21} (diamonds) of a 110 × 75 μm^2 diamond Schottky p-i-n diode from 1 to 25 GHz for DC bias from 0 to 7.5 V in 0.5 V steps. The simulated values are shown as a solid line for S_{11} and a dashed line for S_{21} The Smith chart is normalized for $Z_0 = 50$ Ω.

forward bias of 1 V before entering the sub-exponential regime at 3 V. In contrast, a true p-i-n diode with an undepleted phosphorus doped n-type layer of thickness 530 nm required > 4 V to enter the exponential current regime [12]. To confirm that the n-type region of the diode used for this work is fully depleted we have plotted the energy band diagram using Silvaco ATLAS TCAD (Technology Computer Aided Design) simulations, see Fig. 5. The simulations are based on the approach described in [35] and use an incomplete ionization model for the dopant impurities, a constant activation energy for the phosphorus donors, and a concentration dependent activation for the boron acceptors. The parameters used for the simulation are summarized in Table 2. The pronounced band bending at the surface of the diode confirms that the 50 nm thick n-type layer is fully depleted. As can be seen from the band diagram the barrier to hole transport, ϕ_p, is 2.2 eV while the energy required for electrons to overcome the barrier at x = 0 nm, ϕ_n, is 4.17 eV. As a result, current transport across a Schottky p-i-n diode is unipolar, and in this case due solely to the thermionic emission of holes [34].

After calibration of the GSG probes using an impedance standard substrate the 2-port S-parameters of the diode were measured from

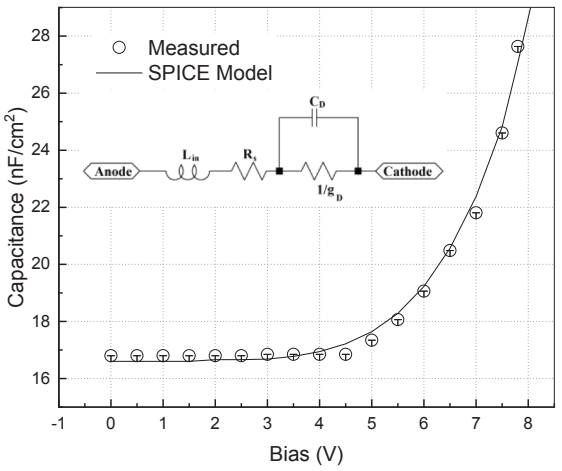

Fig. 7. The capacitance (open circles) of the Schottky p-i-n diode is extracted as a function of bias by fitting the *RLC* model (shown in the inset) to the Z-parameters derived from the measured S-parameters in Fig. 6. The solid line is the fit to the compact model *C(V)* equation developed in Section 5.

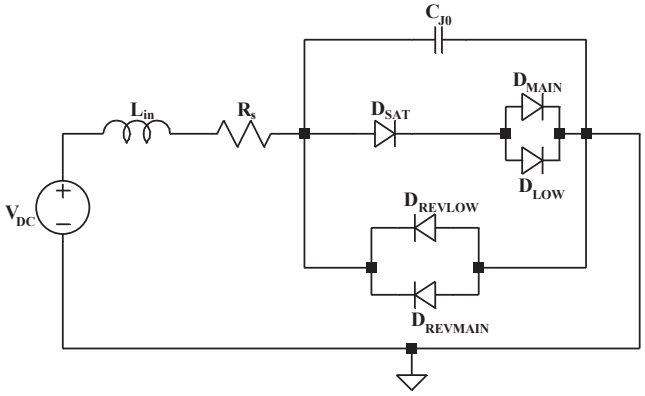

Fig. 8. Compact model sub-circuit for the Schottky p-i-n diode. The extracted component values for each of the diodes are given in Table 3. The constant depletion capacitance, C_{J0}, is 1.4 pF for the 110 × 75 μm^2 diode used here while the series resistance, R_s, is 1.6 Ω. For completeness, a series inductor, L_{in} = 15 pH is included in the model, and is required to fit the data at high frequencies. igure 9: The magnitude (circles) and phase (squares) of (a) the return loss, S_{11}, and (b) the insertion loss S_{21}, of the diamond Schottky p-i-n diodes as a function of forward bias, at a frequency of 1 GHz. The solid and dashed lines are the fits to the corresponding data derived from the lumped element sub-circuit model of Fig. 8.

100 MHz to 25 GHz. The p-i-n diodes are 2-terminal devices such that $S_{11} = S_{22}$ and $S_{21} = S_{12}$ and the Smith chart in Fig. 6 plots S_{11} and S_{21} for a range of DC forward biases. From the S-parameter data, the corresponding Z-parameters were extracted (not shown) using standard formulas. The impedance data was then used to fit the simple lumped-element RC circuit in the inset to Fig. 7, using the Keysight parameter extraction software, IC-CAP [36]. In this way the total diode capacitance, C_D, can be determined as a function of bias. The resulting CV curves are shown in Fig. 7 and are used to extract the diode model capacitance parameters. At zero bias the capacitance of the diode is 16.8 nF/cm^2, and for a relative permittivity of 5.7 would correspond to an i-layer of thickness 300 nm, in excellent agreement with the target growth thickness.

5. Lumped-Element diode model and parameter extraction

Numerical TCAD simulations of the diamond p-i-n diodes provide

Table 3
Diode model parameters used for the sub-circuit of Fig. 8.

	D_{LOW}	D_{MAIN}	D_{SAT}	D_{REVLOW}	$D_{REVMAIN}$
I_S (A)	2.05×10^{-20}	6.06×10^{-20}	9.55×10^{-3}	2.96×10^{-19}	2.39×10^{-21}
n	8.28	3.01	34.6	29.4	23.8
r_S (Ω)	0.001	0.001	0.001	0.001	0.001
TT (ps)	0	0	1.4	0	0

insight into the physical transport mechanisms responsible for the current flow [34,35]. However, they are not practical for simulating circuits with more than a handful of active components, and instead, lumped-element SPICE models are used. Here we demonstrate a SPICE model that accurately reproduces the non-ideal characteristics of the diamond p-i-n diodes with a widely-used sub-circuit approach described in [37]. The sub-circuit is shown in Fig. 8 and uses individual ideal diode models to reproduce different regimes of the measured I-V curves. Each of the diodes in the sub-circuit employs the standard SPICE model with the diode current, I_D, given by (1). By adjusting the saturation current, I_{Sat}, and ideality factor, n, for each diode, an adequate fit to the DC characteristic is achieved as shown by the solid lines in Fig. 4.

$$I_D = I_{Sat}\left(exp\left(\frac{q(V_D - I_D r_s)}{nkT}\right) - 1\right) \quad (1)$$

The principal diodes in the sub-circuit are D_{MAIN}, which reproduces the regime from 1 to 3 V where the current increases exponentially, while D_{SAT} reproduces the current from approximately 3 V to < 7 V where the transition from exponential behavior to the quasi-linear regime takes place. The D_{SAT} diode is used to mimic transport mechanisms not captured by Eq. (1), including effects due to non-linear p- and n-type contacts, carrier injection and space-charge conduction. The series resistance, r_s, of the D_{MAIN} and D_{SAT} diodes are set to be vanishingly small at 1 mΩ so that the on-resistance of the p-i-n diode for biases above 7 V is determined by the series resistance component, R_s, which is set at 1.6 Ω.

For reverse bias » 3kT/q Eq. (1) predicts a constant current of -I_{Sat}. To replicate the increasing reverse bias currents observed in the data we again follow reference [37] and use reverse-connected diodes D_{REVLOW} and $D_{REVMAIN}$. The diode D_{REVLOW} models the gradual increase in current from −4V to −9V after which the parallel connected diode $D_{REVMAIN}$ takes over to reproduce the increased exponential slope for reverse biases beyond −9V.

For the bias range −4 V < V_d < 1 V the actual diode current is less than the 50 fA resolution of the Agilent 4156 parameter analyzer corresponding to the observed noise floor of 0.7nA/cm^2. The n and I_S parameters for diode D_{LOW} have been chosen to improve the fit to the data at the transition from the low current noise floor to the exponentially increasing current of D_{MAIN} that occurs at a forward bias of 1 V. The DC and AC parameters for the components in the diode sub-circuit of Fig. 8 are listed in Table 3.

The total capacitance of a junction diode, C_D, is the sum of the depletion capacitance, C_{DEP}, which dominates at low currents, and the diffusion capacitance, C_{DIFF}, that increases rapidly as the diode begins to turn on. Diode SPICE models use the product of transit time, TT, and small signal conductance, g_D, to simulate the diffusion capacitance, while C_{DEP} is derived from the depletion approximation. Both terms are included in the expression for C_D given in eq. (2). From the data in Fig. 7 the diode capacitance is constant below ~ 4 V indicating that the grading coefficient, m, in the depletion capacitance expression is approximately zero. For this reason, the depletion capacitance is represented by a constant value capacitance, C_{J0}, connected between the anode and cathode as shown in the diode sub-circuit of Fig. 8.

$$C_D = C_{DEP} + C_{DIFF} = \frac{C_{J0}}{\left(1 - \frac{V_D}{V_J}\right)^m} + TT \bullet g_D \quad (2a)$$

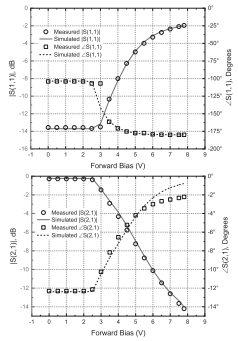

Fig. 9. The magnitude (circles) and phase (squares) of (a) the return loss, S_{11}, and (b) the insertion loss S_{21}, of the diamond Schottky p-i-n diodes as a function of forward bias, at a frequency of 1 GHz. The solid and dashed lines are the fits to the corresponding data derived from the lumped element sub-circuit model of Fig. 8.

$$\approx C_{J0} + TT.g_D \quad (2b)$$

The increase in the total capacitance that is observed in Fig. 7 for V_D > 4 V corresponds with the turn-on voltage of the diode current seen in Fig. 4. In this 'ON' regime the diode conductance, g_D, is controlled by D_{Sat}, before it is ultimately limited by the series resistance, R_s. For the model developed here the diffusion capacitance is therefore associated entirely with diode D_{Sat}, all the other diode transit times being set to zero. As a result, Eq. (2a) can be modified to the simplified form in Eq. (2b) which we use to fit the data in Fig. 7. A junction capacitance, C_{J0}, of 16.8 nF/cm^2 along with a transit time of 1.4 ps for diode D_{Sat} reproduces the total measured diode capacitance, C_D, as shown by the solid line in Fig. 7.

For AC conditions and DC bias V_D > 4 V the diode sub-circuit model of Fig. 8 is consistent with the *RLC* circuit in the inset of Fig. 7. The capacitance of diode D_{Main} is set to zero such that it appears as an AC open circuit. At the same time, very little AC signal is dropped across D_{Main} because the AC current is limited by the conductance of D_{Sat} for V_D > 4 V. As a result, the capacitance of the diode sub-circuit is C_{J0} in parallel with $C_{DIFF} = TT{\cdot}g_D$. The diode capacitance, C_D, of Eq. (2b) is in parallel with the small-signal conductance of D_{Sat}, and the total impedance includes the diode series resistance, R_S.

6. Comparison of measured and simulated S-Parameters

To validate the model, we compare the measured 2-port S-parameters with the simulated results derived using the SPICE netlist for the circuit in Fig. 8. The S-parameters of the p-i-n diodes were recorded using an Agilent 8510C network analyzer with GSG probes from MPI Corporation [38]. The simulated values of S_{11} and S_{21} are plotted in Fig. 6 for a wide range of bias. A series connected inductance, L_{in}, of 15 pH is required to fit the S-parameter measurements at high frequencies, and is attributed to the metallic interconnects used to contact the anode and cathode. The excellent agreement between the measured data and the simulated results confirms the accuracy of the compact model sub-circuit using the set of extracted device parameters shown in Table 3.

When operated as biased controlled attenuators [29] a control voltage is used to switch the diode receiver protector from a low

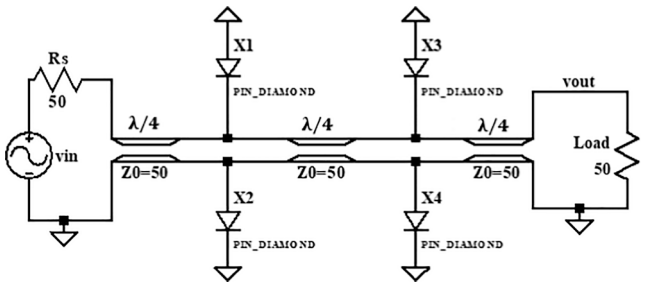

Fig. 10. A 2-stage receiver protector consisting of four identical diamond p-i-n diodes with the sub-circuit of Fig. 8.

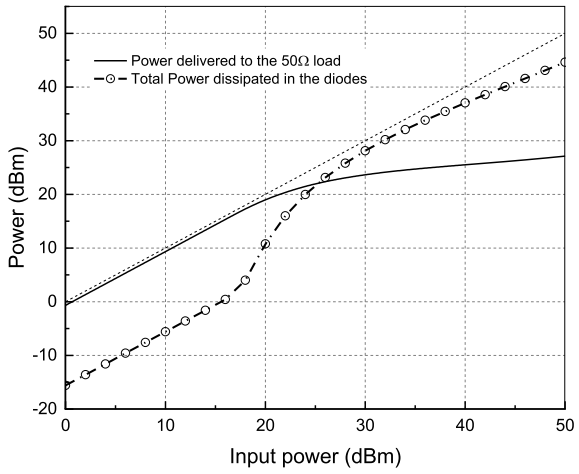

Fig. 11. Simulated output power of the diamond receiver protector of Fig. 10 (solid line) vs. input power. The dashed line with open symbols shows the total power dissipated in the receiver protector circuit.

insertion loss, off-state, to a highly attenuating conducting state, for which the input power is reflected. With two GSG probes placed onto the pads the diode behaves as a shunt attenuator connected between the signal and ground lines of the RF transmission line formed by the GSG probes and the coaxial cables. In this fashion the insertion loss, S_{21}, and the return loss, S_{11}, have been measured as a function of diode voltage for a frequency of 1 GHz, see Fig. 9. The DC diode voltage is applied by means of a bias-T connected to port-1 of the 2-port measurement system. As shown in Fig. 9 the diode shunt contributes <0.3 dB insertion loss until the diode starts to turn on at ~ 2.5 V of forward bias. For the highest bias of 7.8 V at which the 100 mA current compliance occurs, the diode insertion loss is 14 dB and the return loss is −2 dB. The solid lines in Fig. 9 show the simulated magnitude and phase of S_{11} and S_{21} derived from the lumped-element sub-circuit. The good agreement between the measured and simulated insertion loss confirms that the compact model sub-circuit of Fig. 8 is sufficiently accurate for the design of diamond-based receiver protectors such as the two-stage, self-biasing circuit described in Section 7.

7. Simulated 2-Stage diamond Schottky diode receiver protector

In contrast to active, bias-controlled attenuators, passive receiver protectors rely on the self-bias created by a high input power waveform to switch on the diode and reflect the incoming RF power [29,31,39–42]. A back-to-back diode configuration is often employed so that one diode is conducting for the positive input cycle, while the other turns on for negative cycles. A two-stage passive receiver protector such as the one shown in Fig. 10 provides a tradeoff between high power attenuation and circuit complexity.

To evaluate the performance of a diamond-based receiver protector we have used the sub-circuit of Fig. 8 to simulate the power transfer characteristics of the circuit in Fig. 10 operating at 1 GHz. The power delivered to a 50 Ω load as a function of input power is plotted in Fig. 11 along with the total power dissipated in the receiver protector circuit. At input powers above 100 mW the output power starts to be attenuated. For P_{in} = 100 W the power delivered to the load is 0.51 W, with 29 W dissipated in the diodes of the receiver protector and the rest being reflected at the input.

The power dissipated in the diodes of the receiver protector leads to Joule heating, and the resulting increase in temperature will ultimately limit the operation of the receiver protector. It is for these high-power applications that diamond substrates, with their high thermal conductivity, will provide important systems level benefits. To compare the increase in temperature for different substrate materials we use the 1D thermal transport in Eq. (3)

$$\Phi = \kappa A \frac{dT}{dz} \tag{3}$$

where ϕ is the heat flux, K is the thermal conductivity of the substrate, and dT/dz is the temperature gradient in the direction z, normal to the substrate. The diodes in the first stage of the attenuator experience the largest RF voltage swing, and therefore the highest power dissipation. The power density dissipated in a single diode for a temperature drop of 100 °C across a substrate of thickness 300 μm is estimated using eq. (3) with the room temperature thermal conductivities appropriate for silicon, GaAs, SiC and diamond. The values are included in Table 4 along with other key materials parameters for receiver protectors made from these materials. At elevated temperatures the thermal conductivity of the substrates decreases with increasing temperature [43–46] making it harder to dissipate the heat generated in the diodes. As a result, the power densities in Table 4 are an over-estimate, and the devices would experience a temperature increase >100 °C. Nonetheless, the data in Table 4 confirms that compared to other semiconductor material systems diamond-based p-i-n diodes are ideally suited for high power RF receiver protector applications.

8. Conclusions

The DC and AC characteristics of diamond Schottky p-i-n didoes have been measured and used to extract a lumped element compact model. The model accurately reproduces the measured insertion and return loss up to 25 GHz. A passive 2-stage diode limiter circuit, simulated at a frequency of 1 GHz, provides receiver input protection up to 100 W

Table 4
Comparison of diode limiter circuits for different semiconductor materials.

Reference	Material System	Frequency (GHz)	Insertion Loss (dB)	P_{in} for 3 dB attenuation in P_{out} (dBm)	Thermal Conductivity at 300 K ($W{\cdot}cm^{-1}{\cdot}K^{-1}$)	Power Density for ∇T = 100 °C (dBm/mm^2)
[41]	Silicon	3	<1	~20	1.5 [44]	47
[31]	GaAs	10	1.5	~20	0.46 [45]	42
[29]	GaAs	10	0.74	~18	0.46 [45]	42
[39]	GaAs	9.5	<1	~18	0.46 [45]	42
[42]	4H-SiC	2–7	1.1–2.6	Not reported	2.8 [46]	50
This work	Diamond	1	0.3	~25	>20 [43]	58

(50 dBm) of input power. At such high input powers significant diode self-heating is expected, increasing the risk of device failure. The high thermal conductivity of the diamond substrates ensures that the self-heating in diamond-based receiver protectors is kept to a minimum compared to other semiconductor device materials such as silicon, GaAs, and SiC.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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