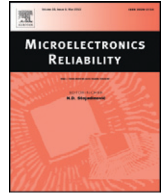
Microelectronics Reliability 63 (2016) 201–213

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr



Band diagram for low-k/Cu interconnects: The starting point for understanding back-end-of-line (BEOL) electrical reliability

Michael J. Mutch [a], Thomas Pomorski [a], Brad C. Bittel [a,b], Corey J. Cochrane [c], Patrick M. Lenahan [a,c,*], Xin Liu [d], Robert J. Nemanich [d], Justin Brockman [e], Marc French [e], Markus Kuhn [e], Benjamin French [f], Sean W. King [e,*]

[a] Intercollege Program of Materials, The Pennsylvania State University, University Park, PA 16802, USA
[b] Quality and Reliability, Intel Corporation, Hillsboro, OR 97124, USA
[c] Department of Engineering Science and Mechanics, The Pennsylvania State University, University Park, PA 16802, USA
[d] Department of Physics, Arizona State University, Tempe, AZ 85287, USA
[e] Logic Technology Development, Intel Corporation, Hillsboro, OR 97124, USA
[f] Ocotillo Materials Laboratory, Intel Corporation, Chandler, AZ 85248, USA

ARTICLE INFO

Article history:
Received 11 January 2016
Received in revised form 12 April 2016
Accepted 18 April 2016
Available online 6 May 2016

Keywords:
Low-k
Interconnect
Band diagram
XPS
EPR
Magnetic resonance

ABSTRACT

The starting point for describing the electrostatic operation of any semiconductor device begins with a band diagram illustrating changes in the semiconductor Fermi level and the alignment of the valence and conduction bands with other interfacing semiconductors, insulating dielectrics and metal contacts. Such diagrams are essential for understanding the behavior and reliability of any semiconductor device. For metal interconnects, the band alignment between the metal conductor and the insulating intermetal and interlayer dielectric (ILD) is equally important. However, relatively few investigations have been made. In this regard, we have investigated the band alignment at the most common interfaces present in traditional single and dual damascene low-k/Cu interconnect structures. We specifically report combined X-ray photoelectron spectroscopy and reflection electron energy loss spectroscopy (REELS) measurements of the Schottky barrier present at the ILD and dielectric Cu capping layer (CCL) interfaces with the Ta(N) via/trench Cu diffusion barrier. We also report similar measurements of the valence and conduction band offsets present at the interface between a-SiN(C):H dielectric CCLs and low-k a-SiOC:H ILDs (porous and non-porous). The combined results point to metal interfaces with the CCL having the lowest interfacial barrier for electron transport. As trap and defect states in low-k dielectrics are also important to understanding low-k/Cu interconnect reliability, we additionally present combined electron paramagnetic resonance (EPR) and electrically detected magnetic resonance (EDMR) measurements to determine the chemical identity and energy level of some electrically active trap/defect states in low-k dielectrics. Combined with the photoemission derived band diagrams, the EPR/EDMR measurements point to mid-gap carbon and silicon dangling bond defects in the low-k ILD and CCL, respectively, playing a role in electronic transport in these materials. We show that in many cases the combined band and defect state diagrams can explain and predict some of the observed reliability issues reported for low-k/Cu interconnects.

© 2016 Elsevier Ltd. All rights reserved.

1. Introduction

As the nano-electronics industry continues dimensional scaling into the single digit nanometer regime in a relentless pursuit to maintain Moore's Law [1–3], back-end-of-line (BEOL) interconnect performance and reliability are becoming increasingly important [4–7]. In contrast to transistors where Dennard dimensional scaling leads to significant gains in transistor performance [8], dimensional scaling of the interconnect leads to increases in important basic metrics such as resistance and capacitance that can degrade the interconnect and overall integrated device performance [9,10]. To minimize these negative effects, insulating materials with increasingly lower values of dielectric constant (i.e. low-k) are being explored and implemented in order to reduce interconnect resistance–capacitance delays and capacitive power dissipation [11–14]. However, the higher electrical leakage [15] and reduced dielectric breakdown strength [16] exhibited by low-k materials are serious reliability concerns [17–21] — particularly as electric fields approach 1 MV/cm or greater for <10 nm technologies due to lack of voltage scaling [22].

Much of the physics describing electrical leakage, breakdown, and other reliability problems in classic electro-static semiconductor devices can be captured in band diagrams which illustrate changes in semiconductor Fermi level/doping and the alignment of the valence and conduction bands of the semiconductor with other interfacing semiconductors,

* Corresponding authors.
E-mail addresses: pmlesm@engr.psu.edu (P.M. Lenahan), sean.king@intel.com (S.W. King).

http://dx.doi.org/10.1016/j.microrel.2016.04.004
0026-2714/© 2016 Elsevier Ltd. All rights reserved.

insulating dielectrics and metal contacts [23,24]. These band diagrams can also be utilized to describe the same types of leakage and dielectric breakdown reliability issues that are present for metal interconnect and other capacitive structures [25–27]. Unfortunately, relatively little is known regarding the interfacial band alignment between materials that comprise the current state-of-the-art low-*k*/Cu interconnects utilized in the nano-electronics industry. The few published studies of the fundamental electronic band alignment in low-*k*/metal interconnects have focused primarily on the interface between the Ta/TaN via/trench Cu diffusion barrier and the low-*k* a-SiOC:H interlayer dielectric (ILD) that serves as the insulator preventing line-to-line leakage between Cu conductors in the same metal interconnect layer (see Fig. 1(a)) [28,29]. Electron transport across this interface, however, represents only one possible leakage path in a low-*k*/Cu interconnect [30, 31]. As shown in Fig. 1(b), line-to-line leakage can also occur via electron transport through the Cu capping layer (CCL) near the CCL/low-*k* ILD interface due to the presence of Ta/TaN "dog ears" created by differences in local chemical mechanical polish rates for the Ta/TaN barrier versus Cu and the low-*k* ILD [32,33]. Similarly, layer–layer leakage can occur across the Cu CCL/ILD interfaces (see Fig. 2).

In this regard, we have performed a combined X-ray photoelectron spectroscopy (XPS) and reflection electron energy loss spectroscopy (REELS) study to determine the valence and conduction band offsets (VBO and CBO) present at all the interfaces in state-of-the-art low-*k*/Cu interconnect structures. In this article, we summarize prior results looking at the low-*k* CCL/Cu [34,35] and low-*k* CCL/ILD [36] interfacial band alignment, and present new results investigating the band alignment at Cu/low-*k* ILD interfaces and interfaces between Ta(N) and both the low-*k* CCL and ILD. We combine all these results to present a complete band diagram for providing an initial physical description of some of the basic electrical reliability issues associated with low-*k*/Cu interconnect structures.

As point defects and traps of any kind are also essential to understanding the reliability physics of both semiconductor devices and metal interconnect structures, we additionally summarize and review prior work utilizing primarily electron paramagnetic resonance (EPR) to determine the chemical identity of some of the dominant defects present in typical low-*k* CCL and ILDs [37–47]. We then combine these

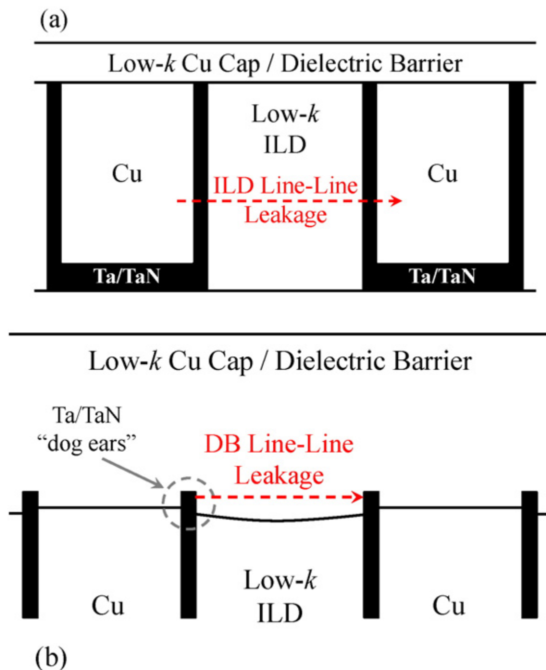


Fig. 1. Schematic diagram illustrating two possible line–line leakage paths through (a) the low-*k* ILD, and (b) the low-*k* Cu Cap / Dielectric Barrier (DB).

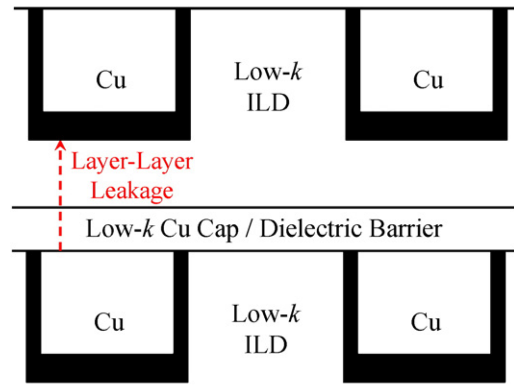


Fig. 2. Schematic diagram illustrating the interfaces that must be traversed for layer–layer electrical leakage in a typical low-*k*/Cu interconnect structure.

results with defect energy levels determined using ultra-violet spectroscopic ellipsometry (UVSE), REELS, and newly developed electrically detected magnetic resonance (EDMR) techniques [48]. As we will show, adding the EPR and EDMR results to the above band diagram leads to a more complete description of the physics for some of the electrical reliability issues associated with low-*k*/Cu interconnects.

2. Experimental

2.1. XPS Φ_B and ΔE_v measurements

The a-SiO_2, a-SiO_xC_y:H, and a-SiC_xN_y:H thin films utilized in this study were all deposited on 300 mm diameter Si (100) wafers by plasma enhanced chemical vapor deposition (PECVD) using standard commercially available tools [49,50]. Deposition temperatures for the a-SiO_2, a-SiCN:H, and non-porous a-SiOC:H thin films were on the order of 400 °C. The process gases utilized included various silane, methlysilane, and methylsiloxane like sources diluted in gases such as N_2, H_2, NH_3, He, N_2O, O_2, and CO_2 [51–53]. Deposition of porous a-SiOC:H ILD materials was performed at lower temperatures (~250 °C) using a sacrificial organic pore-building "porogen" in combination with the preceding precursors [54]. A post-deposition electron beam or UV cure at ~400 °C was utilized to remove the second phase organic porogen [55]. Table 1 summarizes some of the key material properties for the a-SiO_2, a-SiO_xC_y:H, and a-SiC_xN_y:H, films investigated in this study including nominal composition, dielectric constant, refractive index, mass density, and bandgap (E_g). The bandgap measurements were performed using REELS and have been previously described in detail [56,57]. Additional details concerning the thin films, PECVD processing and material property measurements have been previously reported elsewhere [58].

The Ta thin films were deposited on 300 mm diameter Si (100) wafers by standard physical vapor deposition (PVD) methods using a commercially available tool [59]. The TaN films were deposited by reactive PVD using N_2 as the nitrogen source and working gas [60]. After deposition, the Ta(N) films were transferred ex-situ to the PECVD tool for deposition of the previously mentioned low-*k* dielectric films.

The method of Grant and Waldrop was utilized to determine the Schottky barrier at the low-*k* ILD and CCL interfaces with Cu and Ta(N) [61]. This method relies on referencing the core levels of the dielectric to the valence band maximum and then measuring how the position of the core levels change at the interface with the metal of interest. Specifically:

$$\Phi_B = E_g - (E_{CL})_{int} + (E_{CL} - E_v)_{bulk}, \tag{1}$$

where Φ_B is the Schottky barrier at the dielectric/metal interface, E_g is the bandgap of the dielectric, $(E_{CL})_{int}$ is the dielectric core level energy

Table 1
Summary of properties for PECVD a-SiO_2, low-*k* a-SiO_xC_y:H, and low-*k* a-SiC_xN_y:H thin films investigated in this study. RI = refractive index at 673 nm.

Film	k (±0.1)	RI (±0.001)	Density (g/cm^3)	Porosity (%)	E_g (eV)	ILD or Cu Cap
a-SiO_2	4.2	1.46	2.3 ± 0.1	0	8.8 ± 0.14	ILD
a-$SiO_{1.7}C_{0.8}$:H	3.2	1.44	1.6 ± 0.1	0	8.2 ± 0.14	ILD
a-$SiO_{1.6}C_{1.5}$:H	3.0	1.43	1.3 ± 0.1	0	8.2 ± 0.14	ILD
a-$SiO_{1.6}C_{1.5}$:H	2.8	1.41	1.2 ± 0.1	0	8.2 ± 0.14	ILD
a-$SiO_{1.7}C_{0.8}$:H	2.5	1.33	1.2 ± 0.1	25 ± 5	8.2 ± 0.14	ILD
a-$SiO_{1.6}C_{1.5}$:H	2.3	1.33	0.9 ± 0.1	33 ± 5	7.8 ± 0.14	ILD
a-$SiC_{0.7}O_{0.6}$:H	4.8	1.77	2.0 ± 0.1	0	3.1 ± 0.14	CCL
a-SiC:H	6.5	2.34	2.5 ± 0.1	0	2.7 ± 0.14	CCL
a-$SiC_{0.6}N_{0.5}$:H	5.8	2.0	2.25 ± 0.1	0	3.2 ± 0.14	CCL
a-SiN:H	6.5	2.0	2.5 ± 0.1	0	3.2 ± 0.14	CCL

at the interface (relative to the Fermi level), and $(E_{CL} - E_v)_{bulk}$ is the position of the dielectric core level relative to the valence band maximum (VBM) measured at least 10 nm away from any interfaces. For these measurements, the Si 2p core level was used to determine $(E_{CL})_{int}$ and $(E_{CL} - E_v)_{bulk}$ [34,35].

To determine the valence band offset (VBO) at interfaces between a-SiO_xC_y:H ILDs and a-SiC_xN_y:H CCLs, both indirect and direct techniques employing XPS were utilized. The indirect core level referencing method of Kraut [62] was utilized first to determine the valence band offset (VBO) at the a-SiC_xN_y:H/a-SiO_xC_y:H interfaces and has been previously described in detail [63–65]. The method relies on referencing distinct core levels (CL) in the two dielectric materials to their respective valence band maxima (VBM) and then measuring the relative position of these core levels with respect to one another at their interface, as per:

$$\Delta E_v\ (\mathrm{SiCN:H/SiOC:H}) = (E_{CL} - E_V)_{SiOC} - (E_{CL} - E_V)_{SiCN} + \Delta(E_{CL})_{int}, \quad (2)$$

where ΔE_v is the valence band offset between the two materials and $\Delta(E_{CL})_{int}$ is the relative position of the core levels in the two materials at the interface i.e. $\Delta(E_{CL})_{int} = [(E_{CL})_{SiN} - (E_{CL})_{SiOC}]_{int}$. Additional attempts were also made to determine the VBO directly from valence band spectra of the a-SiC_xN_y:H/a-SiO_xC_y:H interface and will be described in more detail in a following section.

For both the Φ_B and ΔE_v measurements, an H_2 plasma pre-treatment was performed in-situ prior to deposition of the a-SiC_xN_y:H DB on Ta or the low-*k* a-SiOC:H ILD in order to emulate typical low-*k* interconnect processing [66,67]. Such plasma pre-treatments are commonly performed prior to low-*k* CCL deposition on Cu interconnects in order to remove Cu corrosion inhibitors and surface oxides left behind by the Cu CMP process [68,69], and to improve the electromigration [70,71], time dependent dielectric breakdown (TDDB) [72,73], and adhesion performance of the low-*k* CCL interfaces with Cu and the low-*k* ILD [74,75].

After PECVD deposition, the dielectric samples were transferred ex-situ to a VG Theta 300 XPS system equipped with a hemispherical electron energy analyzer and a monochromated Al anode X-ray source (1486.6 eV) [34–36]. The peak positions for all the XPS core levels were determined via curve fitting using Casa XPS software [76]. The VBM was determined via linear regression analysis of the steepest slope of the turn on in photoemission in the XPS valence band spectra [77].

2.2. EPR and EDMR measurements

Conventional EPR measurements utilized a Bruker X-band spectrometer with a 300 series bridge, a transverse electric 104 microwave cavity and a weak pitch standard [37–39]. EDMR measurements were performed at room temperature at multiple field/frequency combinations over a range of dielectric biasing conditions. X-band EDMR measurements were carried out at room temperature utilizing a custom built spectrometer consisting of a 4 in. Lakeshore electromagnet, a Resonance Instruments 8330 series X-band microwave bridge with a transverse electric 102 microwave cavity. The electromagnet was controlled by a Lakeshore 475 DSP Gaussmeter with a remote computer interface [48]. To accurately measure magnetic fields, a nuclear magnetic resonance (NMR) Gaussmeter was utilized. Low-field EDMR measurements were performed on home-built EDMR spectrometers. The low-field EDMR spectrometers utilized homemade nested Helmholtz coils. The low-frequency RF magnetic field is supplied by a Stanford Research Systems signal generator and a Doty Scientific RF coil and tuned circuit. The test structures utilized in EDMR measurements were Al/Ti/low-*k* dielectric/p-Si capacitors fabricated by shadow masked electron beam evaporation of first 10 nm of Ti followed by 1 μm of Al on blanket low-*k* films of varying thickness. The size of the circular Ti/Al top electrodes ranged from 0.020 to 0.080″ diameter.

Multiple frequency EDMR measurements were made to overcome the limited structural information available from the essentially featureless EDMR spectra observed in this study. By making measurements at multiple frequencies and considering the role of spin-orbit coupling in determining the line widths in magnetic resonance spectra, some additional insight into defect structure can be gained. A brief explanation of rudimentary magnetic resonance concepts is provided here to support further discussion of the EDMR results. For an array of identical defects, in the simplest of cases, the resonance condition may be expressed as:

$$h\nu = g\beta H. \quad (3)$$

Here, h is Planck's constant, ν is the RF or microwave frequency, β is the Bohr magneton, H is the applied magnetic field, and g is an orientation dependent value which may be expressed as a second rank tensor. For a randomly oriented array of identical defects with axial symmetry, for example dangling bonds, resonance is observed over a range of magnetic field and, if the line width is entirely due to g, the line width is given by [78]:

$$\Delta H \approx \frac{h\nu}{4\beta}\left|g_{\perp} - g_{||}\right|, \quad (4)$$

where $g_{\perp}$ ($g_{||}$) satisfies the resonance condition when the magnetic field is perpendicular (parallel) to the axis of symmetry of the defect. This expression requires that $g_{\perp} \approx g_{||} \approx 2$, a reasonable approximation for silicon and carbon dangling bonds. (In general, g is expressed as a second rank tensor; in an axially symmetric case, there are only two values for the tensor parameters, $g_{\perp}$ and $g_{||}$.) The essential point here is that the line width expressed in Eq. (4) is proportional to frequency, and to the range of g values. Additional factors, in these samples, primarily electron-nuclear hyperfine interactions, may also contribute to line width; however, to zeroth order, hyperfine interaction to the line widths are independent of the frequency of measurement whereas the g contribution to line width should approximately follow expression (4). Thus, a comparison of high and very low frequency EDMR traces should allow for a rough calculation of the range of g values.

In simple dielectric systems, the presence of a single defect, very nearly identical at each site, may dominate the resonance response. However, in disordered systems, such as low-*k* dielectrics, EPR (and thus EDMR) spectra are likely dominated by defects, such as carbon or silicon dangling bonds which might exhibit modest site to site differences. These site to site differences along with hyperfine interactions from nearby but not precisely identical sites of magnetic nuclei lead to the observation of broad, featureless spectra, making defect identification difficult. However, by utilizing multiple frequency EDMR measurements, we can get a rough calculation of the range of *g* tensor components by utilizing expression (4) and making measurements at high and very low frequencies. The Δg is directly related to spin orbit coupling, and thus charge within the nucleus, and the orbital angular momentum of the electrons involved in the paramagnetic defect [79]. All things being equal, larger (smaller) measurements of Δg are likely a result of larger (smaller) central atoms. (This is not inevitably the case, but the results should provide some general guidance with respect to defect identification.) One would expect a larger range of *g* tensor components for a silicon dangling bond than for a carbon dangling bond. For carbon dangling bonds in amorphous carbon, theoretical predictions have suggested $\Delta g \approx 0.0009$ [80]. This is in agreement with the prior high/low frequency EDMR measurements on a-C:H by the authors that indicated $\Delta g = 0.0010 \pm 0.0004$ [81]. EPR measurements and theoretical calculations in a-Si:H have indicated that, for silicon dangling bonds in these systems, $\Delta g \approx 0.004$ [82]. Such findings are in agreement with the authors' baseline high/low frequency EDMR measurements in a-Si:H films, which yield $\Delta g = 0.0041 \pm 0.0004$ [81].

3. Results and discussion

3.1. Line–line leakage: Low-k ILD/Ta(N) and Cu band alignment

Prior studies of the fundamental electronic band alignment in low-*k*/metal interconnects have focused primarily on Cu/Ta(N)/low-*k* a-SiOC:H interfaces where (as shown in Fig. 1a) the low-*k* dielectric serves as the insulator preventing line–line leakage between Cu conductors in the same metal interconnect layer [28,29]. This prior work used internal photoemission techniques (IPE) and focused primarily on SiO_2 and a-SiOC:H dielectrics with *k* values in the range of 2.4–3.0. In this section, we utilize XPS to look at a slightly lower $k = 2.3$, 33% porous a-SiOC:H dielectric (see Table 1 for additional material properties). In Fig. 3, we present the XPS valence band spectrum acquired from a 200 nm thick version of the $k = 2.3$ a-SiOC:H film. As previously described [36], electrostatic charging was observed during the XPS measurement of this film and the presented XPS spectrum was charge-corrected by 5.4 eV to align the O 2 s peak position to 25.7 eV, matching the value previously measured from a thin SiO_2 film deposited on Cu. Please note that this charge shift did not affect the binding energy difference between the Si 2p core level and the VBM, which is the quantity needed for the band alignment calculation. As shown in Fig. 3, the valence band maximum in this spectrum was located at 4.6 ± 0.1 eV using linear regression analysis. Fig. 4(a) shows the corresponding spectrum of the Si 2p core level from the same film with the same charge correction as in Fig. 3. The Si 2p spectrum in Fig. 4(a) was fit well to a single Gaussian–Lorentzian line shape and the peak position was determined to be 103.4 eV. The corresponding value of Si2p–VBM was determined to be 98.8 ± 0.1 eV.

In Fig. 4(b), we show the Si 2p core level measured from a TaN/$k = 2.3$ a-SiOC:H dielectric interface formed by depositing 5 nm of TaN on 200 nm of the $k = 2.3$ a-SiOC:H. Since the TaN film as-deposited was too thick to detect the Si 2p core level from the underlying a-SiOC:H dielectric, in-situ Ar^+ sputtering was used to thin the TaN layer until the Si 2p core level from the a-SiOC:H dielectric was detected with a sufficient signal to noise ratio. The Si 2p peak position for the TaN/a-SiOC:H interface was determined to be 102.85 ± 0.03 eV using again a single Gaussian–Lorentzian line-shape with a Shirley background and without any charge correction (i.e. the overlying TaN layer was sufficiently conductive to prevent any observable surface charging). Combining this value with Si2p–VBM $= 98.8 \pm 0.1$ eV and the bandgap of 7.8 ± 0.2 eV previously determined by REELS [56], Eq. (1) gives a Schottky barrier of 3.75 ± 0.2 eV. For a similarly prepared 5 nm pure Ta/$k = 2.3$ a-SiOC:H interface, identical XPS measurements indicated a Schottky barrier of 3.8 ± 0.2 eV. These values are in excellent agreement with the prior IPE measurements of higher *k* a-SiOC:H dielectrics where barriers of 3.9–4.5 eV were determined for Ta(N)/a-SiOC:H interfaces [28,29].

Due to the need to reduce the high resistance of the Ta/TaN via/trench barrier for future <10 nm technologies [83], aggressive thickness scaling of the Ta/TaN barrier has been pursued [84], as well as alternative self forming (SF) barriers that eliminate the Ta/TaN barrier completely [85]. For both scenarios, knowledge of the band alignment at a Cu/low-*k* ILD interface is needed due to possible lack of continuity in either the Ta/TaN or SF barrier layers. Therefore, similar measurements to those described above were performed by depositing 3 nm of a previously described $k = 3.2$ a-SiOC:H ILD [65] directly on a 300 nm Cu film and measuring the position of the Si 2p core level which was determined to be 103.2 eV. Using the previously determined value of 99.8 eV for Si2p–VBM and $E_g = 8.2$ eV [65], the Schottky barrier for this interface was determined to be 4.7 ± 0.2 eV. This value is consistent with prior IPE measurements of ~4.5 eV for the Schottky barrier at Au/low-*k* ILD interfaces [28]. It is also in excellent agreement with the value of 4.8 ± 0.1 determined by Guo et al. via vacuum ultraviolet photoemission spectroscopy of a similar a-SiOC:H/Cu interface [86].

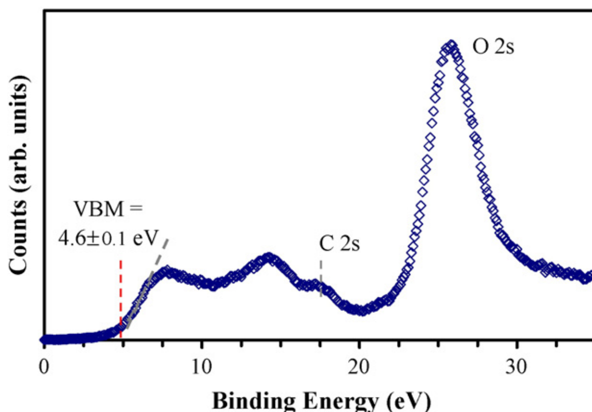


Fig. 3. XPS valence band spectrum of $k = 2.3$ a-SiOC:H ILD.

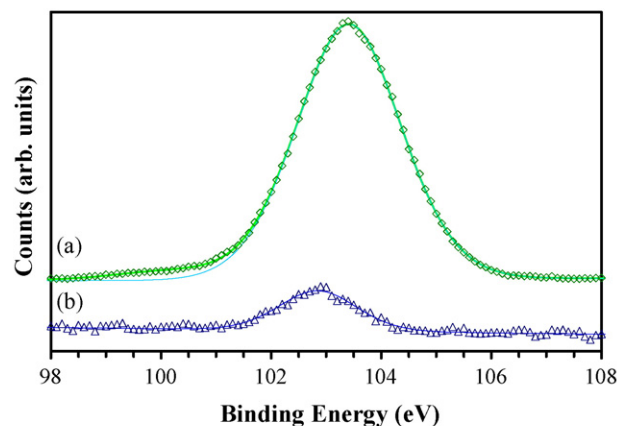


Fig. 4. XPS spectrum of Si 2p core level from (a) $k = 2.3$ a-SiOC:H ILD and (b) a TaN/Ta interface with the same $k = 2.3$ a-SiOC:H ILD.

3.2. Line–line leakage: low-k CCL/Ta(N) band alignment

As shown in Fig. 1(b), an alternate line–line leakage path exists through the low-*k* CCL at or near the interface with the low-*k* ILD. This leakage path typically exists due to the presence of Ta(N) barrier "dog ears" that project up above the plane of the Cu and ILD surfaces and are created by differences in the polish/erosion rate of Ta(N) relative to Cu and the low-*k* ILD during the Cu CMP process [32,33]. These Ta(N) dog ears present a possible point for electrons to be injected into the low-*k* CCL instead of the low-*k* ILD [87,88]. Therefore, the band alignment/Schottky barrier present at the low-*k* CCL/Ta(N) interface is an important consideration that has been neglected in many studies of low-*k*/Cu interconnect reliability [28,29].

To determine the Schottky barrier at the low-*k* CCL/Ta(N) barrier interface, the method of Kraut was again utilized. However, this time the low-*k* CCL was deposited directly on a 100 nm Ta film previously deposited on Si. This was done both to eliminate possible charging concerns in the measurements and to simulate typical low-*k*/Cu interconnect fabrication where the low-*k* CCL is deposited after completion of a Cu CMP process that creates and exposes the Ta(N) dog ears in addition to the Cu and low-*k* ILD surfaces. Table 1 summarizes the properties of the low-*k* CCLs investigated in this study which included dense/non-porous a-SiC:H, a-SiCN:H, a-SiN:H, and a-SiOC:H films as well as one $k = 3.2$ a-SiOC:H ILD film for comparison. Table 2 summarizes the Si2p–VBM and Si2p $(E_{CL})_{int}$ values measured for 2–3 nm of these films deposited directly on the 100 nm Ta film. As shown in Table 2, the Schottky barrier determined for the low-*k* CCL/Ta interfaces are all roughly 2 ± 0.2 eV and substantially less than the value of 3.8 eV determined for the $k = 3.2$ a-SiOC:H ILD/Ta interface. The latter value is also in excellent agreement with the value of 3.8 eV determined in the previous section for the Ta(N)/$k = 2.3$ a-SiOC:H interface.

The low-*k* CCL/Ta Schottky barriers are consistent with the previous measurements of the Schottky barrier at low-*k* CCL/Cu interfaces and the intrinsically lower band-gap of the CCL materials. Based on pure band energy alignment considerations, line–line leakage through the CCL or in the CCL/ILD interface seems to be a lower barrier route as opposed to line–line leakage directly through the ILD. This, however, does not consider the presence of defects/traps in the dielectrics that could substantially lower the barriers for electron transport through these materials and will be the subject of following sections.

It should also be noted that despite using an in-situ H_2 plasma pretreatment prior to the low-*k* CCL deposition on the Ta film, a TaO_x surface oxide that formed during air exposure likely remains at the low-*k* CCL/Ta interface. Some evidence for such a TaO_x interfacial layer was gained by examining the Ta 4f of the low-*k* CCL/Ta interfaces investigated in this study. As shown in Fig. 5, chemically shifted Ta $4f_{7/2,5/2}$ peaks at 26 and 28.4 eV were observed in all cases and attributed to Ta–O bonding at the low-*k* CCL/Ta interface. The prominence of these features varied with the CCL and was most prominent for the a-SiOC:H/Ta interfaces where some additional oxidation of the Ta surface likely occurred during the initial stages of a-SiOC:H deposition after the H_2 plasma treatment (see Fig. 5(b)). The enthalpy of formation for Ta_2O_5 is large (−2046 kJ/mol) [89] and thus there is a strong likelihood for Ta to oxidize in the presence of an oxidizing plasma. Similarly, TaO_x surface oxides also exhibit a high thermodynamic stability and are difficult to reduce to a metallic state. This is clearly shown in Fig. 6 where in-situ XPS spectra of the Ta 4f from an oxidized Ta surface is presented (a) before and (b) after exposure to a remote H_2 plasma treatment optimized for cleaning low-*k* ILD and CMP Cu surfaces [66]. The existence of a surface oxide is clearly evident via the presence of chemically shifted Ta–O $4f_{7/2,5/2}$ peaks at 27.5 and 29.4 eV relative to the less intense metallic Ta 4f peaks at 22.4 and 24.2 eV. Comparison of Fig. 6(a) and (b) shows that the remote H_2 plasma treatment had little to no effect on the intensity of the Ta–O $4f_{7/2,5/2}$ peaks despite having previously demonstrated a strong ability to reduce organic and oxide contaminants on low-*k* ILD and Cu surfaces [66]. This clearly indicates that any oxidation of the Ta(N) barrier that occurs during Cu CMP and after air exposure likely remains and is unchanged by the various H_2 and NH_3 plasma pre-treatments utilized in the industry [67,70–75]. As will be discussed later, possible remaining oxidation of the Ta(N) barrier "dog ears" is an important consideration for many low-*k*/Cu reliability issues including line–line leakage, electromigration, and TDDB.

Table 2
Summary of Si2p–VBM, $(E_{CL})_{int}$, and the calculated Schottky barrier (Φ_B) for various low-*k* dielectric interfaces with Ta.

Ta/	Si2p–VBM (eV)	$Si2p_{int}$ (eV)	Φ_B (eV)
$a\text{-}SiO_{1.7}C_{0.8}$:H ($k = 3.2$)	98.7 ± 0.1	103.3 ± 0.05	3.8 ± 0.2
$a\text{-}SiC_{0.7}O_{0.6}$:H ($k = 4.8$)	100.9 ± 0.1	102.2 ± 0.05	1.9 ± 0.2
a-SiC:H ($k = 6.5$)	99.7 ± 0.1	100.4 ± 0.05	1.8 ± 0.2
$a\text{-}SiC_{0.6}N_{0.5}$:H ($k = 5.8$)	100.3 ± 0.1	101.3 ± 0.05	2.0 ± 0.2
a-SiN:H ($k = 6.5$)	100.8 ± 0.1	101.9 ± 0.05	2.1 ± 0.2

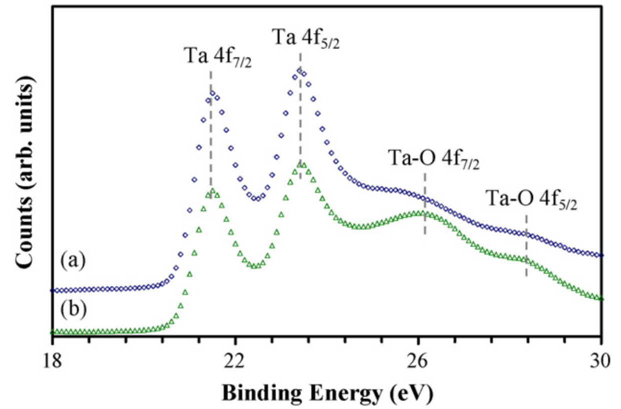


Fig. 5. XPS spectrum of Si 2p core level from (a) $k = 2.3$ a-SiOC:H ILD and (b) a TaN/Ta interface with the same $k = 2.3$ a-SiOC:H ILD.

3.3. Layer–layer leakage: low-k CCL/ILD band alignment

As shown in Fig. 2, a final possible leakage path to consider in low-*k*/Cu interconnects is layer–layer leakage between overlying Cu lines. In this scenario, electrons must traverse not only the Schottky barrier present at the Cu/low-*k* CCL interface, but also the conduction band offset at the low-*k* CCL/ILD interface. As discussed in the preceding sections, we have previously measured the Schottky barrier at low-*k* CCL/Cu interfaces [34,35] and recently also reported on the VBO and CBO at low-*k* a-SiCN:H CCL/a-SiOC:H ILD interfaces [36]. In this article, we present additional results looking in greater detail at the influence of *k*/porosity on

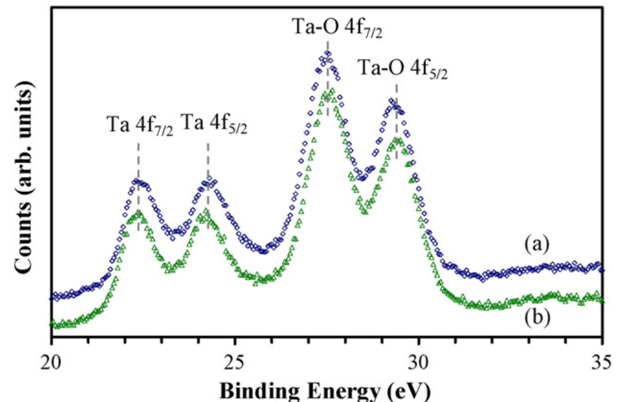


Fig. 6. XPS spectrum of Ta 4f from 100 nm Ta film (a) before and (b) after a remote H_2 plasma clean.

the VBO and CBO at low-*k* a-SiCN:H/a-SiOC:H interfaces, and also investigate the effect of the low-*k* CCL composition by looking at a-SiN:H/a-SiOC:H interfaces.

For the CCL/ILD CBO measurements, XPS was utilized to first determine the interfacial valence band offset and then the conduction band offset was determined using the measured VBO and the bandgap of the dielectrics previously determined using REELS [56,57]. To determine the VBO, we utilized the previously described method of Kraut [62] with the a-SiOC:H ILD VBM being referenced to the O 1s core level and the a-SiCN:H CCL VBM to the N 1s core level. In a previous study [36], the value of O 1s-VBM was determined to be 528.6 ± 0.1 eV for non-porous a-SiOC:H dielectrics, and 528.5 ± 0.1 eV for porous a-SiOC:H dielectrics. Similarly, the value of N 1s-VBM was determined to be 396.5 ± 0.1 eV for the a-SiCN:H dielectric [36]. To measure $(E_{CL})_{int}$, 2–3 nm of a-SiCN:H was deposited on 100–200 nm a-SiOC:H films of varying *k*/porosity and the relative position of the O 1s and N 1s were determined using XPS. These values and the calculated VBO and CBO are summarized in Table 3. These results show that the *k*/porosity of the low-*k* ILD has a relatively small effect on the a-SiCN:H/a-SiOC:H VBO and CBO.

To investigate the influence of the CCL composition on the CCL/ILD band alignment, 2–3 nm of a-SiN:H was deposited on some of the same low-*k* ILDs, and the relative position of the O 1 s and N 1 s core levels was again measured. As shown in Table 4, slightly larger VBOs and smaller CBOs were determined for the a-SiN:H/a-SiOC:H interfaces relative to the a-SiCN:H/a-SiOC:H interfaces.

The VBO at the a-SiN:H/a-SiOC:H interface was also determined directly by depositing 2 nm of the $k = 3.2$ a-SiOC:H dielectric directly on 25 nm of the a-SiN:H on Cu. In this case, it was found that the a-SiOC:H/a-SiN:H interfacial VBO could be determined directly from the XPS valence band spectrum of this interface. As shown in Fig. 7, the VBO of 3.5 ± 0.3 eV determined directly is in excellent agreement with the value of 3.6 ± 0.2 eV determined using the core level referencing method. These results are also in reasonable agreement with the value of 3.05 eV determined by Keister for a-Si_3N_4/a-SiO_2 interfaces [90].

3.4. Complete low-k/Cu interconnect band diagram

In this section, we summarize and combine the above results with our previously reported studies to present a series of schematic flat band diagrams illustrating the barriers for electron transport in the various possible leakage paths described in the Introduction. To illustrate the barriers for line–line leakage, we present in Fig. 8 the band alignment of a low-*k* a-SiCN:H CCL and a-SiOC:H ILD to a Ta(N) Cu barrier. As shown and discussed previously, the Schottky barrier at the a-SiCN:H/Ta(N) barrier is substantially smaller and almost half that for the a-SiOC:H/Ta(N) interface. This strongly suggests that line–line leakage through the low-*k* a-SiCN:H CCL is highly likely and could be the dominant leakage path as has been asserted in other detailed electrical examinations of the leakage paths in low-*k*/Cu interconnects [31].

To illustrate the barriers for layer–layer leakage, we present in Fig. 9 the Schottky barrier present at Cu/low-*k* a-SiCN:H CCL interfaces and the VBO and CBO present at a-SiCN:H CCL/a-SiOC:H ILD interfaces. In this case, the low-*k* a-SiCN:H CCL/Cu Schottky barrier is slightly reduced

Table 3
Summary of $(E_{CL})_{int}$ and the calculated VBO and CBO for various low-*k* a-SiCN:H/a-SiOC:H dielectric interfaces.

a-SiCN:H/	$\Delta(E_{CL})_{int}$ (eV)	VBO (eV)	CBO (eV)
a-SiO_2	134.6 ± 0.03	3.1 ± 0.1	2.4 ± 0.2 [36]
a-$SiO_{1.7}C_{0.8}$:H ($k = 3.2$)	134.9 ± 0.03	2.8 ± 0.1	2.2 ± 0.2
a-$SiO_{1.6}C_{1.5}$:H ($k = 2.8$)	134.7 ± 0.03	2.6 ± 0.1	2.4 ± 0.2
a-$SiO_{1.7}C_{0.8}$:H ($k = 2.5$)	134.9 ± 0.03	2.8 ± 0.1	2.0 ± 0.2 [36]
a-$SiO_{1.6}C_{1.5}$:H ($k = 2.3$)	134.6 ± 0.03	2.6 ± 0.1	2.0 ± 0.2 [36]

Table 4
Summary of $(E_{CL})_{int}$ and the calculated VBO and CBO for various low-*k* a-SiN:H/a-SiOC:H dielectric interfaces.

a-SiN:H/	$\Delta(E_{CL})_{int}$ (eV)	VBO (eV)	CBO (eV)
a-$SiO_{1.7}C_{0.8}$:H ($k = 3.2$)	135.3 ± 0.03	3.6 ± 0.1	1.4 ± 0.2
a-$SiO_{1.6}C_{1.5}$:H ($k = 2.3$)	134.9 ± 0.03	3.3 ± 0.1	1.3 ± 0.2

compared to that for low-*k* a-SiCN:H CCL/Ta(N) interfaces. However as illustrated in Fig. 9, a large CBO of 1.4–2.4 eV at the a-SiCN:H CCL/a-SiOC:H ILD exists that must also be overcome. The effective barrier for layer–layer leakage therefore is roughly the sum of the barriers at the Cu/SiCN:H and a-SiCN:H/a-SiOC:H interfaces and is approximately equal to the Ta(N)/a-SiOC:H barrier of 3.8 eV. This again points to the a-SiCN:H CCL/Ta(N) interface as the point of least resistance for electrical leakage in low-*k*/Cu interconnects.

All of the above interfacial barriers to electron transport are substantial and satisfy the rule of thumb criteria of >1 eV established for the interfacial conduction band offset between Si and the gate oxide dielectric in CMOS transistors [91]. This criterion was established to prevent substantial electrical leakage from the gate electrode into the Si channel. Thus, neither significant line–line nor layer–layer leakage would be expected based on the band alignments shown above. Yet, as described previously, electrical leakage is a growing and significant problem in low-*k*/Cu interconnects.

One limitation of the above band structure diagram is that it effectively considers only Schottky based electrical leakage mechanisms where electron transport occurs due to thermionic emission or field enhanced lowering of the interfacial barrier. However, it is well known that electron transport through an insulating dielectric can be greatly assisted by the presence of trap or defects states with energy levels that reside within the bandgap of the dielectric. In fact, trap/defect related leakage mechanisms such as Frenkel–Poole (FP), variable range hopping (VRH), trap-assisted-tunneling (TAT), and Fowler–Nordheim (FN) tunneling are frequently utilized to describe the current–voltage (IV) characteristics of low-*k* dielectrics and integrated low-*k*/Cu interconnect structures [92–96]. The presence and in-operando creation of trap and defect states has also been attributed to other low-*k*/Cu interconnect reliability issues such as stress induced leakage currents (SILC) and TDDB [97–102].

The presence and density of trap/defect states in low-*k* dielectrics has been reported in a number of prior studies [37–48]. However, relatively few have been successful in definitively identifying both the chemical and structural identity of the trap/defect and the energy level of the trap/defect state within the bandgap of the dielectric. In the following sections, we briefly review the prior literature where the

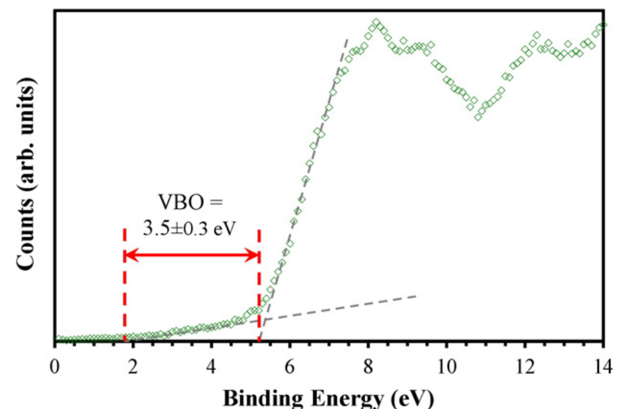


Fig. 7. XPS valence band spectrum illustrating the VBO present at a 2 nm $k = 3.2$ a-SiOC:H/a-SiN:H interface.

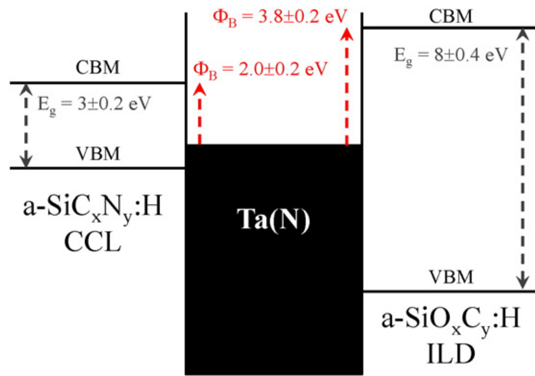


Fig. 8. Schematic flat band diagram illustrating the barrier for electron injection (line–line leakage) from the Ta(N) Cu barrier into either a low-k a-SiOC:H ILD or a low-k a-SiCN:H CCL.

chemical/structural identity of a trap/defect has been identified in a low-k ILD or CCL dielectric and/or the energy position of that defect state has been identified. This review is supported by recent EDMR measurements performed by the authors who definitively demonstrate that electrical leakage through example low-k dielectrics does indeed occur directly through some of the trap/defect states previously identified by EPR. We conclude by updating our previously presented band diagrams with the energy levels established for the identified defect states and attempt to utilize the combined band/defect state diagram to understand reports of electrical leakage and TDDB in several prior low-k/Cu interconnect investigations.

3.5. Low-k ILD defects

Most of what is known concerning the chemical structure of electron trap/defect states in low-k dielectric materials has come from EPR investigations that have identified a variety of unpaired spin (dangling bond) paramagnetic defects associated with either silicon or carbon [37–43,103–106]. One of the earliest studies was reported by Shamuilia et al. where a series of low-k a-SiOC:H ILDs deposited by a variety of methods were investigated and an array of observed silicon dangling bond and vacancy paramagnetic defects were reported [28]. Subsequent studies by multiple other authors have shown that low-k a-SiOC:H dielectrics are sensitive to the creation of a range of additional paramagnetic centers by exposure to UV–VUV radiation, energetic ions, radicals and other forms of ionizing radiation [37–47,103]. Specifically, Bittel [37] and Ren [44,45] have both shown that the density of paramagnetic defect centers in $k = 2.5$–3.0 a-SiOC:H dielectrics can increase by more than an order magnitude due to UV radiation exposure. Additional combined EPR and FTIR studies by Ren showed that exposure of a $k = 2.65$ a-SiOC:H dielectric to an air or N_2 plasma resulted in the creation of silicon dangling bond defects [46].

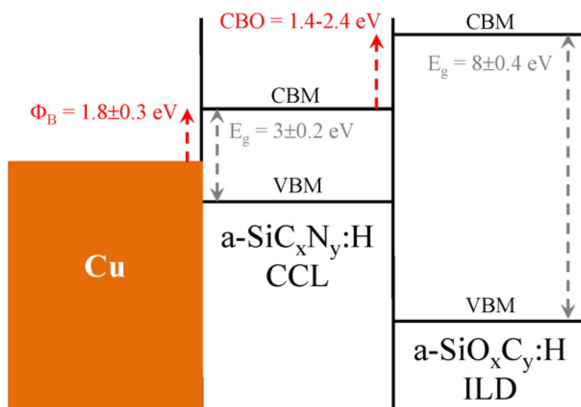


Fig. 9. Schematic flat band diagram illustrating the barrier for electron injection (layer–layer leakage) from Cu across the low-k a-SiCN:H CCL and low-k a-SiOC:H ILD.

EPR studies reported by Afanas'ev have also identified a carbon dangling bond defect state ($g = 2.003$) that they associated with the presence of carbon residues remaining in porous low-k dielectrics due to inefficient removal of the organic porogen utilized to create nanopores in the dielectric [40]. Subsequent studies by Pomorski used the observation of hyperfine splitting due to ^{13}C nuclei to identify carbon dangling bonds as the dominant bulk paramagnetic defect center in both porous low-k a-SiOC:H dielectrics fabricated using an organic porogen and non-porous a-SiOC:H dielectrics that did not utilize an organic porogen [39]. Pomorski also observed a strong correlation between carbon related paramagnetic defects and electrical leakage for both non-porous and porous a-SiOC:H ILD materials [39].

Regarding the energy position of trap/defect states in low-k dielectrics, there have been fewer studies and most, at best, provide a plausible association with one of the specific defect states mentioned above. REELS studies by the authors of porous and non-porous low-k a-SiOC:H dielectrics have identified surface defects states with energy levels of ~5.2 and 7.0 eV created within the a-SiOC:H band-gap by Ar^+ sputtering that were attributed to surface oxygen vacancy (i.e. silicon dangling bond) defect states [56,107]. Theoretical investigations of bulk Si dangling bond defects in SiO_2 indicate that these states occupy a similar energy level in the bulk bandgap [108,109]. Thus, it is plausible to expect Si dangling bonds in the bulk of low-k a-SiOC:H dielectrics to occupy similar energy levels as at the surface.

Regarding carbon related defect states, detailed UVSE and REELS measurements reported by Urbanowicz [40,110] and the authors [56] have both shown that remnants of the organic porogen utilized to create nanoporosity in ultra low-k dielectric materials absorb broadly within the middle of the bandgap of the a-SiOC:H matrix. Although, the authors are unaware of any theoretical calculations regarding carbon or carbon dangling bond related defects in low-k a-SiOC:H or SiO_2 like matrices, a few theoretical investigations of carbon cluster [111,112] and dangling bond defects at SiO_2/SiC interfaces have been reported [113,114]. For C–C pair defects on the SiO_2 side of a SiO_2/SiC interface, these calculations indicate several possible defect states spanning the energy range of 2.5–7.5 eV within the SiO_2 bandgap. These values are roughly in agreement with the values observed by UVSE and REELS for porogen residue defects in ultra low-k a-SiOC:H dielectrics. Recently, Guo has also shown using XPS that Ar^+ sputtering of $k = 2.3$–3.3 a-SiOC:H dielectrics induces surface bandgap narrowing due to the creation of carbon related states 1.3–2.2 eV above the a-SiOC:H VBM [115].

To more definitively establish a correlation between electron transport in low-k a-SiOC:H dielectrics and specific defects, the authors have performed additional variable frequency EDMR measurements on Ti/7 nm $k = 3.2$ a-$SiO_{1.7}C_{0.8}$:H/p-Si capacitor structures. As shown in Fig. 10, the X-band ($\nu = 9.5$ GHz) line width, about 13 G, and zero-crossing $g = 2.0030$ are both within experimental error of conventional X-band EPR measurements in similar systems [39]. The change in measured EDMR line width from X-band to low-frequency is about 3 G, which, utilizing expression (4), yields $\Delta g = 0.0018 \pm 0.0004$. The Δg for the a-$SiO_{1.7}C_{0.8}$:H film, which is within experimental error of Δg measurements in a-C:H via variable frequency EDMR, suggests that the defects responsible for Fig. 10 are carbon dangling bond centers. The nature of EDMR measurements, which are exclusively sensitive to defects involved in transport, directly connects the carbon dangling bonds to electronic transport via spin dependent trap assisted tunneling (SDTAT) or related mechanisms.

To estimate the energy levels of the carbon dangling bond defects in the a-$SiO_{1.7}C_{0.8}$:H system, we compare variable bias EDMR measurements with the band diagram for the a-SiOC:H capacitor structure. Fig. 11 shows EDMR amplitude (ΔI) in a 7 nm a-$SiO_{1.7}C_{0.8}$:H as a function of bias, and Fig. 12 shows the band diagrams for the same structure. For the band diagram simulations, the band gap of the a-$SiO_{1.7}C_{0.8}$:H film was taken to be 8.2 eV, corresponding to prior REELS

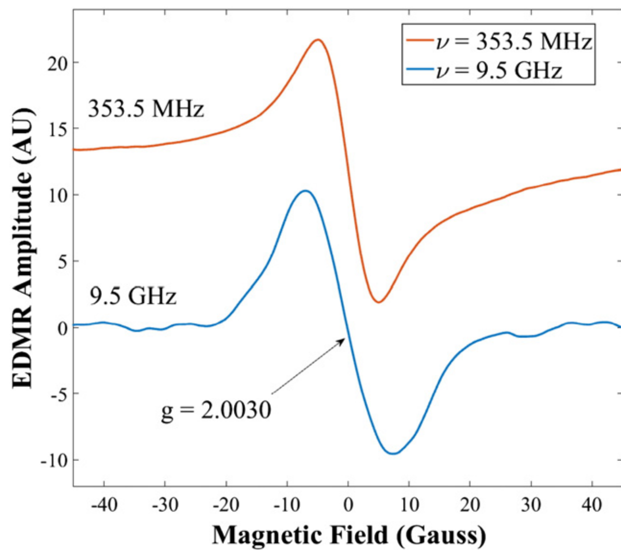


Fig. 10. Variable frequency EDMR in $k = 3.2$, a-$SiO_{1.7}C_{0.8}$:H measurements performed at a bias of −1 V [81]. The magnetic field axes are offset by the EPR centerfield, as defined in Eq. (3). The X-band and low-field peak-to-peak line widths are 13 G and 10 G, respectively. Here, the amplitudes are normalized for comparison. The actual peak-to-peak amplitudes of the responses are about 5 pA.

measurements (see Table 1). Since the Φ_B and VBO for the Ti/a-$SiO_{1.7}C_{0.8}$:H and a-$SiO_{1.7}C_{0.8}$:H/p-Si interfaces are unknown, the reported band alignments for Ti/SiO_2 and SiO_2/p-Si interfaces were used instead [116]. This is partly justified by prior IPE measurements performed by Atkin where the VBO for a $k = 2.4$ a-SiOC:H/Si interface was found to be 4.1 eV, virtually identical to that for a SiO_2/Si interface (4.0 eV) [29].

Note that EPR measurements in these films have indicated that the defect concentration is about 2×10^{17} defects/cm^3. This defect concentration roughly corresponds to an average defect separation of about 15 nm. Thus, we'd expect that tunneling will predominately occur through one defect center through the middle of the a-SiOC:H band gap [117], where tunneling would most effectively occur. In our very crude model, we assume that defects near the middle of the dielectric bandgap dominate transport via trap assisted tunneling. The black circle in each band diagram represents the approximate defect energy levels

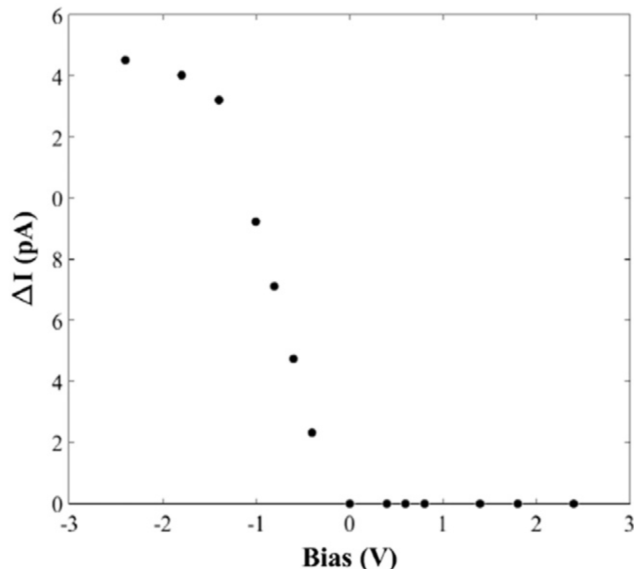


Fig. 11. Variable bias EDMR in a-$SiO_{1.7}C_{0.8}$:H taken at X-band (9.5 GHz). ΔI refers to the peak-to-peak amplitude of the X-band response in Fig. 10.

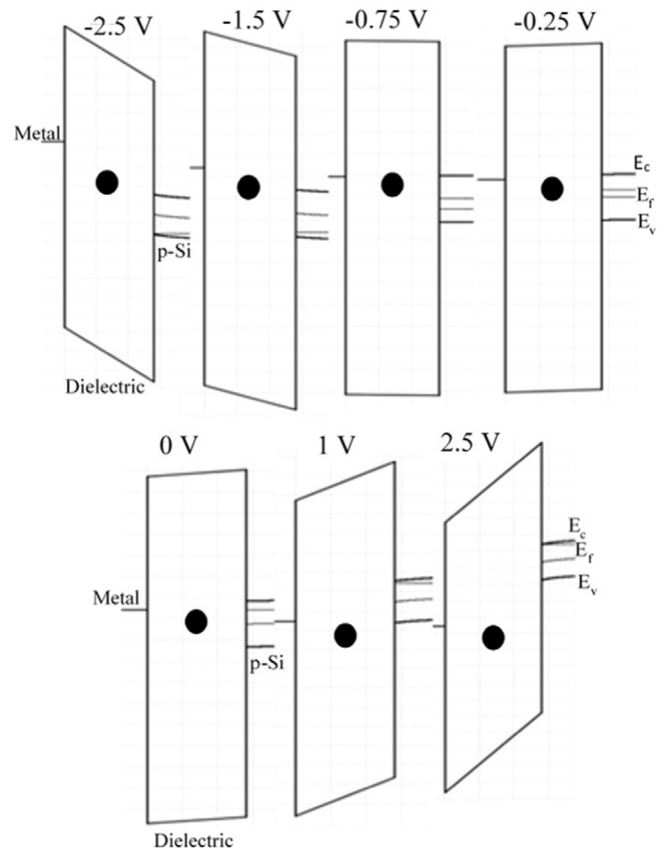


Fig. 12. Simulated band diagrams for the Ti/a-$SiO_{1.7}C_{0.8}$:H/p-Si system at various biases [116]. The band gap of the a-$SiO_{1.7}C_{0.8}$:H dielectric is 8.2 eV. The black dot in the dielectric band gap corresponds to the approximate defect energy levels which we estimate from variable bias EDMR measurements.

which are consistent with the EDMR measurements. It should be emphasized that our analysis of defect energy levels in this study are rather crude, providing only a rough measure of defect energy level locations, rather than exact defect energy levels. Nevertheless, the crude model provides a semi-quantitative explanation of the results, and a rough measure of the defect energy levels. In the case of thicker low-k dielectrics, such as those used for BEOL ILDs, it is likely that the tunneling process would occur through multiple defects. This process is referred to as variable range hopping [118], and has been previously observed in low-k dielectrics [81,119].

Fig. 11 shows that the EDMR response turns on at small negative biases. At these small biases (less than or equal to 750 mV), the band diagrams of Fig. 12 indicate that the metal Fermi energy has not yet crossed the level of the silicon conduction band edge. If the defect levels detected in the EDMR response are located approximately as indicated by the large dot in the Fig. 12 band diagrams, the EDMR response would inevitably be small at such small magnitude negative voltages because the electrons tunneling through the carbon dangling bond defect levels would encounter the very nearly empty silicon band gap. However, as the magnitude of the negative dielectric bias is increased, the metal Fermi level approaches and surpasses the silicon conduction band, allowing for tunneling events through the carbon dangling bonds into abundant states in the silicon conduction band. The ΔI response begins to saturate at about −2.5 V. This likely indicates that the range of defect energy levels is not extremely broad, and suggests the possibility that there may be a diamagnetic level separated by the electron-electron correlation energy. No response is detected at positive biases. At positive biases, the response is not detected because the defect levels are below the metal Fermi energy, and there are no states available for tunneling into the metal. Thus, our multiple frequency

and variable bias EDMR measurements jointly indicate that there are carbon dangling bond centers near the middle part of the a-SiOC:H band gap.

3.6. Low-k CCL defects

Unfortunately, relatively few investigations of trap/defect states in low-k CCL class materials exist. To date, both Kobayashi [120] and Bittel [121] have utilized EPR to investigate paramagnetic defect centers in low-k a-SiCN:H CCLs with k values ranging from 4.8 to 6.5. Both reported paramagnetic defects with g-values that were consistent with silicon dangling bond K centers observed in a-SiN:H. Bittel further showed that the density of Si dangling bond centers and leakage currents in a-SiCN:H both decreased substantially with nitrogen content [121]. The former is consistent with the Si dangling bond assignment, whereas the latter suggests that attention to stoichiometry is important for minimizing both trap/defects and leakage currents in a-SiCN:H CCL films.

For low-k a-SiC:H CCLs, a detailed EPR investigation by Pomorski, in contrast, determined that carbon dangling bond defects were the dominant paramagnetic defects for stoichiometric films [38]. This study also showed a strong correlation between electrical leakage and paramagnetic defects and a strong correlation between hydrogen content and spin defect density. The former is consistent with prior observations for both low-k a-SiOC:H ILDs [39,40] and low-k a-SiCN:H CCLs [32] while the latter correlation is consistent with the ability of hydrogen to passivate dangling bond defects. Interestingly, a strong correlation between sp^2 carbon clusters, EPR carbon dangling bond defects, and electrical leakage has also been observed in bulk polymer derived a-SiC:H and a-SiCN:H ceramics [122–124]. Additional studies have also found low-k CCL materials to be sensitive to creation of additional trap/defect states by exposure to various forms of UV and ionizing radiation [120,121,125].

Fortunately, substantially more is known regarding the energy levels of trap/defect states in a-SiN:H and a-SiC:H CCL materials thanks to several prior studies investigating their properties for use in a variety of non-volatile memory [126], optoelectronic [127], and photovoltaic [128] devices. For stoichiometric a-Si_3N_4, theoretical calculations by Robertson have shown that silicon dangling bonds introduce states in the mid to mid-upper portion of the bandgap, while nitrogen dangling bond states lie within the top of the valence band [129–131]. The presence of non-stoichiometry, as is common in PECVD a-SiN_x:H CCLs, can introduce Si–Si states that lie closer to mid-gap for Si rich stoichiometries and can lead to significant bandgap narrowing for $x < 1.2$ [129–131]. Similarly, N dangling bond states can rise above the valence band maximum for nitrogen rich stoichiometries [129–131]. This picture has largely been confirmed experimentally by a combination of EPR, XPS, and related techniques [132–139].

For stoichiometric a-SiC:H, analogous theoretical calculations by Robertson have shown that Si dangling bond levels similarly lie below the conduction band minimum at ~2 eV within the bandgap [140]. In contrast, sp^3 carbon dangling bond states reside closer to mid-gap at ~0.6–1.2 eV. For non-stoichiometric a-$Si_{1-x}C_x$:H, Si–Si states in Si rich films introduce states just above and below the VBM and CBM, respectively, that effectively lead to bandgap narrowing as carbon content is decreased. For carbon rich a-$Si_{1-x}C_x$:H films, sp^2 carbon clusters are predicted to form that create bonding and anti-bonding states that define the bandgap for $x > 0.6$. As for a-SiN:H, the above picture has also been largely confirmed experimentally by a combination of ESR, XPS, and other techniques [141–147].

To more definitively establish a correlation between electron transport in low-k a-SiCN:H CCL materials and specific defects, we have again performed variable frequency EDMR measurements using Ti/5–10 nm $k = 5.8$ a-$SiC_{0.6}N_{0.5}$:H/p-Si capacitor structures.

EDMR spectra at X-band ($\nu = 9.5$ GHz) and low-frequency ($\nu = 350$ MHz) are shown in Fig. 13. The zero-crossing $g = 2.0027$ is within experimental error of conventional X-band EPR measurements in these systems [148]. The change in line width from X-band to low-frequency is about 8 G, resulting in a $\Delta g = 0.0047 \pm 0.0004$. This Δg is probably too large to be a carbon dangling bond, and is fairly close to multiple frequency EDMR measurements in a-Si:H [81]. Thus, we attribute the EDMR spectra shown in Fig. 13 to silicon dangling bonds. This result strongly indicates that the Si dangling bonds previously detected by Kobayashi [120] and Bittel [121] using EPR are directly involved in electrical transport through a-SiCN:H CCL materials.

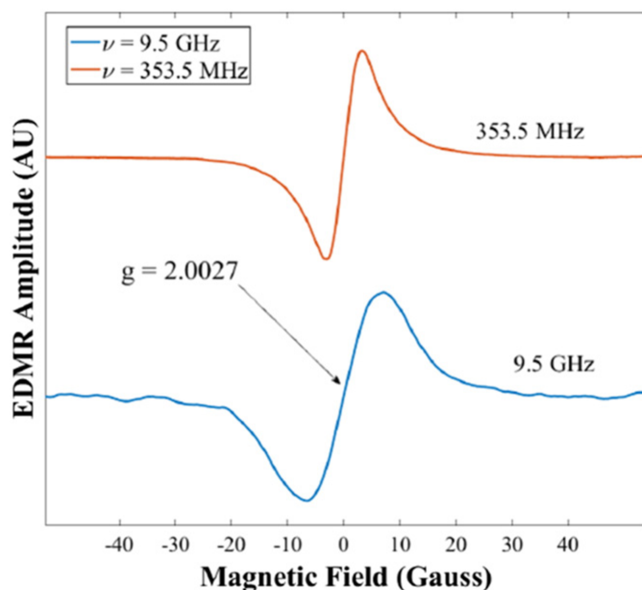


Fig. 13. Variable frequency EDMR in a-SiCN:H measurements performed at a bias of −3 V [81]. The magnetic field axes are offset by the EPR center field, as defined in Eq. (3). The X-band and low-field peak-to-peak line widths are 14 G and 6.1 G, respectively. Here, the amplitudes are normalized for comparison. The actual peak-to-peak amplitudes are about 60 pA.

To estimate defect energy levels in the same $k = 5.8$ a-$SiC_{0.6}N_{0.5}$:H film, we measured ΔI as a function of bias using the same capacitor structures (see Fig. 14). For simulations, the a-$SiC_{0.6}N_{0.5}$:H band gap was taken to be 3.2 eV (see Table 1) and, based on arguments similarly used for Ti/SiOC:H/Si, previous reports for the Ti/SiN:H and SiN:H/Si interfacial band alignments were used. In this case, EDMR was detected at both polarities, but the ΔI response was again anisotropic. The ΔI response was compared with band diagrams that are shown in Fig. 15

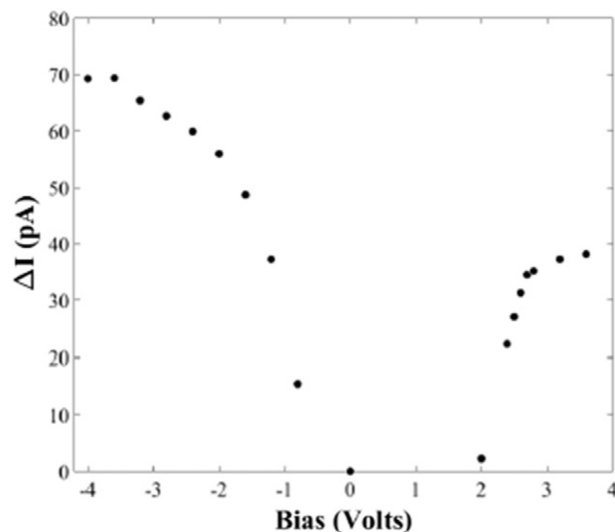


Fig. 14. Variable bias EDMR in a-SiCN:H taken at X-band (9.5 GHz). ΔI refers to the peak-to-peak amplitude of the X-band response in Fig. 13.

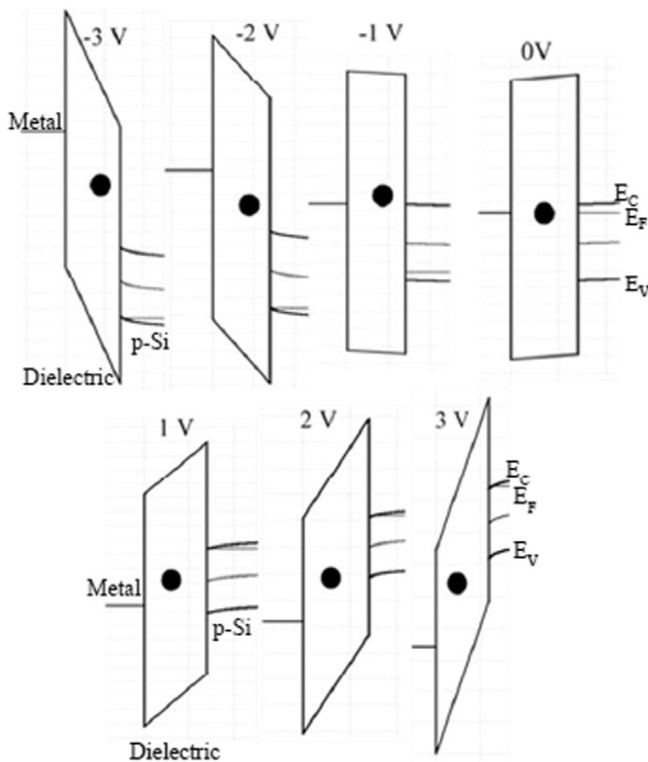


Fig. 15. Simulated band diagrams for the Ti/$k = 5.8$ $SiC_{0.6}N_{0.5}$:H/p-Si system at various biases [116]. The band gap of the $k = 5.8$ $SiC_{0.6}N_{0.5}$:H is 3.2 eV. The black dot in the dielectric band gap corresponds to the approximate defect energy levels we estimate for the measurements.

[116]. As for the case of EDMR in the 7 nm a-SiOC:H film in Section 3.5, one would expect to see the most effective tunneling through just one defect in the middle of the dielectric. In the negative biasing regime, the response is detected at biases as small as -1 V. This is consistent with paramagnetic levels near the middle/upper-middle part of the a-SiCN:H band gap. The black circles in Fig. 15 indicate such levels. The ΔI response increases through biases of roughly -3 V, as the metal Fermi energy is swept through the upper part of the a-SiCN:H band gap.

In the positive biasing regime, the ΔI response does not turn on until about 2 V. At small positive voltages, less than approximately 2 volts, the defect levels are opposite the silicon band gap, as shown in Fig. 15. Thus, there are no states available to provide the tunneling current into the defects. However, when the defect levels cross the silicon valence band maximum, the high density of valence band electrons become available and provides an abundant source of electrons for tunneling through defect levels. The response saturates at both polarities, again suggesting that the defects contributing to the SDTAT do not extend high into the dielectric band gap. These results thus indicate that silicon dangling bond centers with energy levels in the upper part of the band gap play an important role in electrical transport through a-SiCN:H CCL class materials.

3.7. Combined low-k/Cu band and defect diagrams

Having reviewed the variety of different defect and trap states observed in both low-*k* ILD and CCL materials and established a definitive connection between electron transport through these defects via variable bias EDMR, we next update our line–line and layer–layer leakage band diagrams with the rough energy level determined for each class of defect as shown in Figs. 16 and 17, respectively. From Fig. 16, it can be seen that carbon dangling bond and carbon cluster/porogen residue defects in both the low-*k* ILD and CCL layers generally align with the Fermi level of the Ta(N) electrode. Based on this observation, one would anticipate that electrical leakage through either dielectric would likely occur through such defects if present. This is consistent with the EDMR measurements described here on a $k = 3.2$ a-SiOC:H dielectric and prior measurements by Pomorski on low-*k* a-SiC:H CCL class materials [38]. However, for a-SiCN:H CCL materials, EPR and EDMR both point to silicon dangling bonds being more prominent and involved in electrical transport. This indicates that while carbon is present in a-SiCN:H CCL materials, the deposition method and process chemistries utilized must favor conditions that minimize carbon cluster or dangling bond formation and lead instead to a predominance of silicon dangling bond defects.

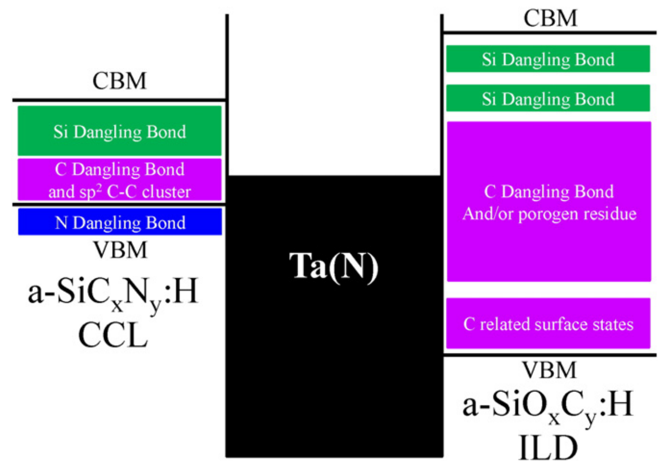


Fig. 16. Schematic flat band diagram (with relevant defect/trap positions added) illustrating the barrier for electron injection (line–line leakage) from the Ta(N) Cu barrier into either a low-*k* a-SiOC:H ILD or a low-*k* a-SiCN:H CCL.

The above defect enriched band alignment diagrams can now be utilized to rationalize the results of several prior investigations of leakage mechanisms in integrated low-*k*/Cu interconnect structures. In many cases, attempts have been made to deduce both the leakage mechanism and interfacial or trap barrier height via a detailed analysis of the current–voltage (IV) characteristics from a low-*k* metal-insulator-metal (MIM) or metal-insulator-semiconductor (MIS) structure [92–96]. In essentially all cases, the barrier heights deduced from the IV analysis have been a small fraction of the IPE or XPS interfacial barrier heights shown above [31]. This discrepancy can now be understood by considering both the dominant trap/defect state likely to be present and its energy level within the low-*k* dielectric.

As one example, Ngwan determined a barrier height of 0.69 eV for trap mediated FP leakage at a a-SiN:H CCL ($k = 6.9$)/a-SiOC:H ILD

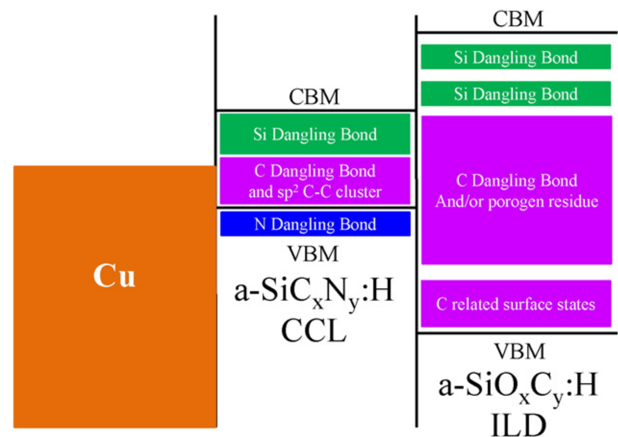


Fig. 17. Schematic flat band diagram (with relevant defect/trap positions added) illustrating the barrier for electron injection (layer–layer leakage) from Cu and across the low-*k* a-SiCN:H CCL and low-*k* a-SiOC:H ILD.

($k = 2.9$) interface in a Cu comb capacitor structure [93]. This barrier height is substantially less then the ~2 eV interfacial Schottky barrier determined by XPS for a-SiN:/Ta interfaces [34]. Based on Fig. 16, the barrier height deduced by Ngwan, however, is consistent with the barrier or trap height that would be expected if electron transport were to occur through the a-SiN:H CCL via Si dangling bond states which as previously discussed have been shown to be the dominant paramagnetic defect in a-SiN:H [127–131]. In this regard, the FP barrier height of 0.69 eV reported by Ngwan is fully consistent with prior investigations of electron transport in PECVD a-SiN_x:H dielectrics where FP leakage with barrier heights of 0.5–1.0 eV have been frequently reported for films with x ranging from 0.5–1.3 [145–147].

As another example, several investigations of electrical leakage in MIM and MIS structures with $k = 2.5$–2.9 ILDs have reported Schottky emission (SE) based leakage with interfacial barrier heights on the order of 0.7–1.0 eV [92–95]. These values are substantially smaller than the interfacial barriers of 4–5 eV determined by XPS and IPE [28,29]. In this case, the greatly reduced interfacial barriers determined electrically can be rationalized by consideration of the likely presence of mid-gap carbon dangling bond defects in the low-*k* ILD. As mentioned previously, several prior studies have established a strong correlation between electrical leakage in low-*k* a-SiOC:H ILDs and the concentration of carbon dangling bond defects or carbon related porogen residues [39,41].

A final and more speculative example concerns the recent investigation by Wu of electrical leakage in a $k = 2.0$, 46% porous a-SiOC:H ILD [96]. In contrast to several prior investigations of lower porosity, $k =$ 2.5–2.9 ILDs where PF leakage has been predominantly reported, Wu observed for the substantially lower *k*, higher porosity ILD an exponential power law current density vs. electric field dependence at fields of 1–4 MV/cm. This dependence was determined to be consistent with a trap limited, space-charge-limited current (SCLC) leakage mechanism. The high exponent of the observed power law dependence was attributed to the filling of an exponential distribution of trap states with the maximum density at the band edge. At fields >5 MV/cm, Wu further observed a transition to trap-assisted tunneling (TAT) followed by Fowler-Nordheim (FN) tunneling. Additional detailed analysis deduced barrier heights of 2.4 and 4.2 eV for TAT and FN leakage, respectively. This distinctive behavior can be understood via consideration of both the unique processing the low-*k* ILD received and the defect enriched low-*k* ILD band diagram shown in Fig. 17. For the former, a remote H_2 plasma cure was employed prior to standard UV curing to more efficiently remove the organic porogen and optimize mechanical properties [149]. Prior UVSE measurements reported by Baklanov have shown that porous low-*k* ILDs cured in this manner exhibit zero traces of porogen residues in the bandgap [41]. Further, EPR measurements reported by Pomorski also show a near complete absence of carbon dangling bond defects, and in contrast show a broad defect center that has been tentatively attributed to a Si dangling bond [38]. Thus, the low-field SCLC leakage observed by Wu is consistent with the likely absence of mid-gap carbon related defect states. Also, the high field TAT based leakage with a barrier height of 2.4 eV is consistent with transport through Si dangling bonds where Fig. 11 indicates that these defects should lie at a similar energy level.

3.8. Application of low-k/Cu band diagram

Having established combined band and defect alignment diagrams of general relevance to low-*k*/Cu interconnects and shown a general agreement with prior electrical measurements of trap and interfacial barrier heights, we next attempt to apply these diagrams to still poorly understood reliability issues and identify possible routes to improved low-*k*/Cu interconnect reliability performance. From a quick examination of Figs. 16 and 17, one easy observation is that carbon related defects have energy levels in the mid-bandgap that can effectively lower the barrier for electron transport across any low-*k* ILD or CCL. As additional studies have linked the presence of carbon to other reliability issues such as TDDB [150], this obviously suggests that elimination of such defects (or carbon all together) should significantly reduce leakage currents and generally improve reliability. However, the insertion of carbon via terminal organic groups is necessary for reducing *k* in both ILD and CCL materials by disrupting the base SiO_2 and Si_3N_4 network structure and facilitating the creation of nanoporosity with a $k = 1$ [11,151]. Thus, clever ways are necessary for avoiding the formation of such carbon related defects or removing them after they have formed.

However, for non-porous low-*k* a-SiOC:H dielectrics, the origin of the carbon related defects is less clear and more research will be needed to understand the origin of their formation and to develop clever ways to avoid their occurrence or ameliorate their presence. In this regard, we do note that spin-on deposited low-*k* a-SiOC:H ILDs have been previously observed to generally exhibit reduced concentrations of carbon dangling bond related paramagnetic defects relative to plasma deposited low-*k* a-SiOC:H ILDs [38]. The primary difference between the two deposition methods is that the latter proceeds via electron assisted bond dissociation of radicals and ions that must react and reform bonds on the wafer surface. Thus, the incorporation of unpassivated bonds is likely. Spin-on deposition, however, proceeds via condensation reactions that break and reform chemical bonds in a more coordinated fashion. Thus, deposition methods that promote bond formation may need to be considered in the future in order to achieve improved reliability performance.

A more subtle consideration originating from Figs. 16 and 17 concerns the stoichiometry of the low-*k* CCL and ILD materials. As mentioned previously, the presence of Si–Si defects in a-SiN:H and a-SiC:H can introduce states below the CBM that if present in sufficient quantity (i.e. off stoichiometric) can effectively narrow the bandgap of these dielectrics and thus reduce the interfacial and trap barrier heights for electronic transport [129–134]. Thus, significant attention to detail on low-*k* composition [152], stoichiometry and network chemical structure may be required for optimum electrical, thermal, and mechanical reliability.

To conclude, we note that many more complex phenomena limit the reliability performance of low-*k*/Cu interconnects that are not covered in the defect enriched band diagrams of Figs. 16 and 17 such as hydrogen [101], moisture [153–156], Ta [157,158], and Cu [159–162] catalyzed failures. Consideration of such effects is beyond the scope of this article, but represents an important area of future research in low-*k*/Cu interconnect reliability. However, it is hoped that the defect enriched band diagrams established in this article will provide an improved platform for developing a completely physics based understanding of low-*k*/Cu interconnect reliability.

4. Conclusions

In summary, we have utilized XPS and REELS to determine the band alignment at various interfaces present in low-*k*/Cu interconnect structures. The combined measurements have allowed us to create a series of band diagrams illustrating the interfacial barriers for both line–line and layer–layer leakages in low-*k*/Cu interconnects. Examination of these combined diagrams points to metal/CCL interfaces as having the lowest barriers for electronic transport and could thus represent likely leakage paths. However, defects can effectively reduce barriers for electronic transport and we have therefore further enriched the diagrams by providing the plausible energy levels for various trap/defect states in low-*k* ILD and CCLs based on REELS, UVSE, EDMR and other reported measurements. The enriched diagrams point to mid-gap carbon and silicon dangling bonds in the low-*k* ILD and CCL layers, respectively, as the mostly likely defect/trap states to be involved in electronic transport. By reviewing several prior studies, we have demonstrated that the combined band alignment and defect energy level diagrams allow many reported electrical leakage mechanisms and reliability issues in low-*k* dielectrics and integrated low-*k*/Cu interconnects to be understood in greater detail. It is hoped that the defect enriched band diagrams

established in this article will provide an improved platform for understanding of low-*k*/Cu interconnect reliability and become a physics based platform to understanding other hydrogen, moisture, and metal catalyzed reliability failures in greater detail.

Acknowledgments

The authors would like to acknowledge the support and encouragement from Drs. B. Tufts, J. Maiz, B. Boyanov, and J. Clarke of Intel Corporation during the course of this research. Work at The Pennsylvannia State University was supported directly by Intel Corporation. Work at Arizona State University was supported by the Semiconductor Research Corporation through Grant No. P11678.

References

[1] G. Moore, Proc. IEEE 86 (1998) 82.
[2] K. Kuhn, Microelectron. Eng. 88 (2011) 1044.
[3] S. King, H. Simka, D. Herr, H. Akinaga, M. Garner, APL Mater. 1 (2013) 040701.
[4] B. Li, T. Sullivan, T. Lee, D. Badami, Microelectron. Reliab. 44 (2004) 365.
[5] M. Hussein, J. He, IEEE Trans. Semicond. Manuf. 18 (2005) 69.
[6] W. van Driel, Microelectron. Reliab. 47 (2007) 1969.
[7] F. Chen, O. Bravo, D. Harmon, M. Shinosky, J. Aitken, Microelectron. Reliab. 48 (2008) 1375.
[8] R. Dennard, F. Gaensslen, H. Yu, V. Rideout, E. Bassous, A. LeBlanc, IEEE J. Solid State Circuits 9 (1974) 256.
[9] P. Kapur, G. Chandra, J. McVittie, K. Saraswat, IEEE Trans. Electron Devices 49 (2002) 598.
[10] M. Tada, N. Inoue, Y. Hayashi, IEEE Trans. Electron Devices 56 (2009) 1852.
[11] K. Maex, M. Baklanov, D. Shamiryan, F. Iacopi, S. Brongersma, Z. Yanovitskaya, J. Appl. Phys. 93 (2003) 8793.
[12] W. Volksen, R. Miller, G. Dubois, Chem. Rev. 110 (2010) 56.
[13] G. Antonelli, G. Jiang, R. Shaviv, T. Mountsier, G. Dixit, K. Park, I. Karim, W. Wu, H. Shobha, T. Spooner, E. Soda, E. Liniger, S. Cohen, J. Demarest, M. Tagami, O. Vander Straten, F. Baumann, Microelectron. Eng. 92 (2012) 9.
[14] A. Grill, S. Gates, T. Ryan, S. Nguyen, D. Priyadarshini, Appl. Phys. Rev. 1 (2014) 011306.
[15] E. Van Besien, M. Pantouvaki, L. Zhao, D. De Roest, M. Baklanov, Zs. Tokei, and G. Beyer, Microelectron. Eng. 92 (2012) 59.
[16] K. Vanstreels, I. Ciofi, Y. Barbarin, M. Baklanov, J. Vac. Sci. Technol. B 31 (2013) 050604.
[17] J. Llyod, E. Liniger, T. Shaw, J. Appl. Phys. 98 (2005) 84109.
[18] G. Haase, J. Appl. Phys. 105 (2009) 44908.
[19] F. Chen, M. Shinovsky, IEEE Trans. Electron Devices 56 (2009) 2.
[20] F. Chen, M. Shinovsky, J. Appl. Phys. 108 (2010) 054107.
[21] C. Wu, Y. Li, M. Baklanov, K. Croes, ECS J. Solid State Sci. Technol. 4 (2015) N3065.
[22] S. Borkar, IEEE J. Lightwave Technol. 31 (2013) 3927.
[23] A. Grove, E. Snow, B. Deal, C. Sah, J. Appl. Phys. 35 (1964) 2458.
[24] A. Kerber, E. Cartier, IEEE Trans. Device Mater. Reliab. 9 (147) (2009).
[25] J. Simmons, Phys. Rev. 155 (1967) 657.
[26] J. Yeargan, H. Taylor, J. Appl. Phys. 39 (1968) 5600.
[27] M. Lenzlinger, E. Snow, J. Appl. Phys. 40 (1969) 278.
[28] S. Shamuilia, V. Afanas'ev, P. Somers, A. Stesmans, Y. Li, Z. Tokei, G. Groeseneken, K. Maex, Appl. Phys. Lett. 89 (2006) 202909.
[29] J. Atkin, D. Song, T. Shaw, E. Cartier, R. Laibowitz, T. Heinz, J. Appl. Phys. 103 (2008) 094104.
[30] K. Yeap, M. Gall, Z. Liao, C. Sander, U. Muehle, P. Justison, O. Aubel, M. Hauschildt, A. Beyer, N. Vogel, E. Zschech, J. Appl. Phys. 115 (2014) 124101.
[31] F. Chen, M. Shinosky, Microelectron. Reliab. 54 (2014) 529.
[32] J. Noguchi, N. Konishi, Y. Yamada, IEEE Trans. Electron Devices 52 (2005) 934.
[33] D. Wang, W. Wang, M. Huang, A. Lek, J. Lam, Z. Mai, AIP Adv. 4 (2014) 077124.
[34] S. King, M. French, M. Jaehnig, M. Kuhn, B. Boyanov, B. French, J. Vac. Sci. Technol. B 29 (2011) 051207.
[35] S. King, M. French, M. Jaehnig, M. Kuhn, B. French, Appl. Phys. Lett. 99 (2011) 202903.
[36] S. King, J. Brockman, M. French, M. Jaehnig, M. Kuhn, B. French, J. Appl. Phys. 116 (2014) 113703.
[37] B. Bittel, P. Lenahan, S. King, Appl. Phys. Lett. 97 (2010) 063506.
[38] T. Pomorski, B. Bittel, C. Cochrane, P. Lenahan, J. Bielefeld, S. King, J. Appl. Phys. 114 (2013) 074501.
[39] T. Pomorski, B. Bittel, P. Lenahan, E. Mays, C. Ege, J. Bielefeld, D. Michalak, S. King, J. Appl. Phys. 115 (2014) 234508.
[40] V. Afanas'ev, K. Keunen, A. Stesmans, M. Jivanescu, Z. Tokei, M. Baklanov, G. Beyer, Microelectron. Eng. 88 (2011) 1503.
[41] M. Baklanov, L. Zhao, E. Besien, M. Pantouvaki, Microelectron. Eng. 88 (2011) 990.
[42] V. Afanas'ev, A. Nguyen, M. Houssa, A. Stesmans, Z. Tokei, M. Baklanov, Appl. Phys. Lett. 102 (2013) 172908.
[43] J. Lauer, H. Sinha, M. Nichols, G. Antonelli, Y. Nishi, J. Shohet, J. Electrochem. Soc. 157 (2010) G177.
[44] H. Ren, M. Nichols, G. Jiang, G. Antonelli, Y. Nishi, J. Shohet, Appl. Phys. Lett. 98 (2011) 102903.
[45] H. Ren, Y. Nishi, J. Shohet, Electrochem. Solid-State Lett. 14 (2011) H107.
[46] H. Ren, G. Jiang, G. Antonelli, Y. Nishi, J. Shohet, Appl. Phys. Lett. 98 (2011) 252902.
[47] H. Sinha, H. Ren, M. Nichols, J. Lauer, M. Tomoyasu, N. Russell, G. Jiang, G. Antonelli, N. Fuller, S. Engelmann, Q. Lin, V. Ryan, Y. Nishi, J. Shohet, J. Appl. Phys. 112 (2012) 111101.
[48] C. Cochrane, P. Lenahan, Appl. Phys. Lett. 104 (2014) 093503.
[49] S. King, J. Vac. Sci. Technol. A 29 (2011) 041501.
[50] Y. Matsuda, S. King, J. Bielefeld, J. Xu, R. Dauskardt, Acta Mater. 60 (2012) 682.
[51] S. King, D. Jacob, D. Vanleuven, B. Colvin, J. Kelly, M. French, J. Bielefeld, D. Dutta, M. Liu, D. Gidley, ECS J. Solid State Sci. Technol. 1 (2012) N115.
[52] Y. Matsuda, S. King, R. Dauskardt, Thin Solid Films 531 (2013) 552.
[53] E. Andideh, M. Lerner, G. Palmrose, S. El-Mansy, T. Scherban, G. Xu, J. Blaine, J. Vac. Sci. Technol. B 22 (2004) 196.
[54] S. Bailey, E. Mays, D. Michalak, R. Chebiam, S. King, R. Sooryakumar, J. Phys. D. Appl. Phys. 46 (2013) 045308.
[55] V. Jousseaume, A. Zenasni, L. Favennec, G. Gerbaud, M. Bardet, J. Simon, A. Humbert, J. Electrochem. Soc. 154 (2007) G103.
[56] S. King, B. French, E. Mays, J. Appl. Phys. 113 (2013) 044109.
[57] B. French, S. King, J. Mater. Res. 28 (2013) 2771.
[58] S. King, J. Bielefeld, G. Xu, W. Lanford, Y. Matsuda, R. Dauskardt, N. Kim, D. Hondongwa, L. Olasov, B. Daly, G. Stan, M. Liu, D. Dutta, D. Gidley, J. Non-Cryst. Solids 379 (2013) 67.
[59] K. Yin, L. Chang, F. Chen, J. Kai, C. Chiang, G. Chuang, P. Ding, B. Chin, H. Zhang, F. Chen, Thin Solid Films 388 (2001) 27.
[60] R. Hubner, M. Hecker, N. Mattern, V. Hoffmann, K. Wetzig, C. Wenger, H. Engelmann, C. Wenzel, E. Zschech, J. Bartha, Thin Solid Films 437 (2003) 248.
[61] J. Waldrop, R. Grant, Y. Wang, R. Davis, J. Appl. Phys. 72 (1992) 4757.
[62] E. Kraut, R. Grant, J. Waldrop, S. Kowalczyk, Phys. Rev. Lett. 44 (1980) 1620.
[63] S. King, R. Davis, C. Ronning, M. Benjamin, R. Nemanich, J. Appl. Phys. 86 (1999) 4483.
[64] S. King, R. Davis, C. Ronning, R. Nemanich, J. Electron. Mater. 28 (1999) L34.
[65] S. King, M. Paquette, J. Otto, A. Caruso, J. Brockman, J. Bielefeld, M. French, M. Kuhn, B. French, Appl. Phys. Lett. 104 (2014) 102901.
[66] X. Liu, S. Gill, F. Tang, S. King, R. Nemanich, J. Vac. Sci. Technol. B 30 (2012) 031212.
[67] F. Ito, H. Shobha, M. Tagami, T. Nogami, S. Cohen, Y. Ostrovski, S. Molis, K. Maloney, J. Femiak, J. Protzman, T. Pinto, E. Ryan, A. Madan, C. Hu, T. Spooner, Microelectron. Eng. 92 (2012) 62.
[68] Y. Hong, D. Eom, S. Lee, T. Kim, J. Park, A. Busnaina, J. Electrochem. Soc. 151 (2004) G756.
[69] S. Govindaswany, A. Tripathi, I. Suni, Y. Li, J. Electrochem. Soc. 155 (2008) H459.
[70] A. Vairagar, S. Mhaisalkar, A. Krishnamoorthy, Thin Solid Films 462 (2004) 325.
[71] T. Usui, H. Miyajima, H. Masuda, K. Tabuchi, K. Watanabe, T. Hasegawa, H. Shibata, Jap. J. Appl. Phys. 45 (2006) 1570.
[72] C. Hsu, D. Perng, W. Lin, K. Lu, T. Tsai, C. Huang, J. Wu, J. Electrochem. Soc. 158 (2011) H1133.
[73] J. Noguchi, N. Ohashi, T. Jimbo, H. Yamaguchi, K. Takeda, K. Hinode, IEEE Trans. Electron Devices 48 (2001) 1340.
[74] S. Chang, Y. Huang, Microelectron. Eng. 85 (2008) 332.
[75] H. Tsai, Y. Chang, S. Chang, Microelectron. Eng. 85 (2008) 1658.
[76] CasaXPS. Casa XPS Software Ltd. 2005.
[77] R. List, W. Spicer, J. Vac. Sci. Technol. B 6 (1988) 1228.
[78] J. Weil, Electron Paramagnetic Resonance: Elemental theory and practical applications, Wiley-Interscience, New York, 1994.
[79] W. Gordy, Theory and Applications of Electron Spin Resonance, Wiley-Interscience, New York, 1980.
[80] N. Ishii, M. Kumeda, T. Shimuzu, Jpn. J. Appl. Phys., Part 2 20 (1981) L673.
[81] M. Mutch, P.M. Lenahan, S.W. King, J. Appl. Phys. 119 (2016) 094102.
[82] M. Stutzmann, D.K. Biegelsen, Phys. Rev. B 40 (1989) 9834.
[83] E. Eisenbraun, Microelectron. Eng. 92 (2012) 67.
[84] C. Liu, W. Liu, Y. Wang, Y. Wang, Z. An, Z. Song, K. Xu, Microelectron. Eng. 98 (80) (2012).
[85] J. Bogan, A. McCoy, R. O'Connor, P. Casey, C. Byrne, G. Hughes, Microelectron. Eng. 130 (2014) 46.
[86] X. Guo, D. Pei, H. Zheng, S. King, Y. Lin, H. Fung, C. Chen, Y. Nishi, J. Shohet, Appl. Phys. Lett. 107 (2015) 232905.
[87] J. Noguchi, T. Oshima, N. Konishi, K. Ishikawa, K. Sato, S. Uno, S. Hotta, T. Saito, H. Aoki, IEEE Trans. Electron Devices 51 (2004) 2168.
[88] C. Hu, L. Gignac, R. Rosenberg, Microelectron. Reliab. 46 (2006) 213.
[89] HSC Thermochemistry 7.0 database. Outotec Research 2006.
[90] J. Keister, J. Rowe, J. Kolodziej, H. Niimi, T. Madey, G. Lucovsky, J. Vac. Sci. Technol. B 17 (1999) 183.
[91] J. Robertson, Rep. Prog. Phys. 59 (2006) 327.
[92] K. Yiang, W. Yoo, Q. Guo, A. Krishnamoorthy, Appl. Phys. Lett. 83 (2003) 524.
[93] V. Ngwan, C. Zhu, A. Krishnamoorthy, Appl. Phys. Lett. 84 (2004) 2316.
[94] M. Vilmay, D. Roy, F. Volpi, J. Chaix, Microelectron. Eng. 85 (2008) 2075.
[95] R. Wang, K. Chang-Liao, T. Wang, M. Chang, C. Wang, C. Lim, C. Lee, C. Chiu, K. Wu, Thin Solid Films 517 (2008) 1230.
[96] C. Wu, Y. Li, Y. Barbarin, I. Ciofi, K. Croes, J. Bommels, I. De Wolf, Z. Tokei, Appl. Phys. Lett. 103 (2013) 032904.
[97] J. Atkin, E. Cartier, T. Shaw, J. Lloyd, R. Laibowitz, T. Heinz, Microelectron. Eng. 86 (2009) 1891.
[98] J. Borja, J. Plawsky, T. Lu, H. Bakhru, W. Gill, J. Appl. Phys. 115 (2014) 084107.
[99] B. Tang, K. Croes, Y. Barbarin, Y. Wang, R. Degraeve, Y. Li, M. Toledano-Luque, T. Kauerauf, J. Bommels, Z. Tokei, I. De Wolf, Microelectron. Reliab. 45 (2014) 1675.
[100] S. Ogden, J. Borja, J. Plawsky, T. Lu, K. Yeap, W. Gill, J. Appl. Phys. 118 (2015) 124102.
[101] C. Wu, Y. Li, I. Ciofi, T. Kauerauf, J. Bommels, I. De Wolf, Zs. Tokei, and K. Croes, J. Appl. Phys. 117 (2015) 064101.

[102] C. Wu, Y. Li, A. Lesniewska, O. Varela, J. Pedreira, D. Marneffe, I. Ciofi, P. Verdonck, M. Baklanov, J. Bommels, I. De wolf, Z. Tokei, K. Croes, J. Appl. Phys. 118 (2015) 164101.
[103] M. Petkov, K. Lynn, K. Rodbell, W. Volksen, R. Miller, IEEE Trans. Nucl. Sci. 49 (2002) 2724.
[104] S. Nakao, Y. Kamigaki, J. Ushio, T. Hamada, T. Ohno, M. Kato, K. Yoneda, S. Kondo, N. Kobayashi, Jpn. J. Appl. Phys. 46 (2007) 3351.
[105] K. Tanbara, Y. Kamigaki, J. Electrochem. Soc. 157 (2010) G95.
[106] D. Griscom, J. Non-Cryst. Solids 352 (2006) 2601.
[107] F. Bart, M. Gautier, J. Duraud, M. Henriot, Surf. Sci. 274 (1992) 317.
[108] E. O'Reilly, J. Robertson, Phys. Rev. B 27 (1983) 3780.
[109] A. Rudenko, F. Keil, M. Katsnelson, A. Lichtenstein, Phys. Rev. B 84 (2011) 085438.
[110] A. Urbanowicz, K. Vanstreels, D. Shamiryan, S. De Gendt, M. Baklanov, Electrochem. Solid-State Lett. 12 (2009) H292.
[111] M. Narisawa, F. Funabiki, A. Iwase, F. Wakai, H. Hosono, J. Am. Ceram. Soc. 98 (2015) 3373.
[112] M. Narisawa, S. Watase, K. Matsukawa, T. Kawai, Y. Kawamoto, T. Matsui, A. Iwase, J. Non-Cryst. Solids 391 (2014) 1.
[113] J. Knaup, P. Deak, T. Frauenheim, A. Gali, Z. Hajnal, W. Choyke, Phys. Rev. B 72 (2005) 115323.
[114] F. Devynck, A. Alkauskas, P. Broqvist, A. Pasquarello, Phys. Rev. B 84 (2011) 235320.
[115] X. Guo, H. Zheng, S. King, V. Afanas'ev, M. Baklanov, J. de Marneffe, Y. Nishi, J. Shohet, Appl. Phys. Lett. 107 (2015) 082903.
[116] R. Southwick III, W.A. Sup, A. Jain, W. Knowlton, IEEE Trans. Device Mater. Reliab. 11 (2011) 236.
[117] R. Wang, S. King, C. Williams, Appl. Phys. Lett. 105 (2014) 052903.
[118] N.F. Mott, Metal-Insulator Transitions, second ed. Taylor & Francis, London, 1990.
[119] B. McGowan, J. Lloyd, Appl. Phys. Lett. 105 (2014) 252902.
[120] K. Kobayashi, H. Yokoyama, M. Endoh, Appl. Surf. Sci. 254 (2008) 6222.
[121] B. Bittel, T. Pomorski, P. Lenahan, S. King, E. Mays, 30th IEEE International Integrated Reliability Workshop Final Report, 2011 50–54.
[122] S. Trassl, G. Motz, E. Rossler, G. Ziegler, J. Non-Cryst. Solids 293 (2001) 261.
[123] K. Wang, X. Li, B. Ma, Y. Wang, L. Zhang, L. An, Appl. Phys. Lett. 104 (2014) 221902.
[124] K. Wang, X. Li, B. Ma, M. Zhang, J. Liu, Y. Wang, L. Zhang, L. An, J. Am. Ceram. Soc. 98 (2015) 2153.
[125] J. Huran, P. Bohacek, V. Shvetsov, A. Kobzev, A. Kleinova, S. Borzakov, L. Hrubcin, M. Sekacova, N. Balalykin, Phys. Status Solidi A 210 (2013) 2756.
[126] S. Fujita, A. Sasaki, J. Electrochem. Soc. 132 (1985) 398.
[127] F. Giorgis, F. Giuliani, C. Pirri, E. Tresso, J. Conde, V. Chu, J. Non-Cryst. Solids 227 (1998) 465.
[128] A. Morimoto, T. Miura, M. Kumeda, T. Shimizu, J. Appl. Phys. 53 (1982) 7299.
[129] J. Robertson, M. Powell, Appl. Phys. Lett. 44 (1984) 415.
[130] J. Robertson, J. Appl. Phys. 54 (1983) 4490.
[131] J. Robertson, Philos. Mag. B 63 (1991) 47.
[132] J. Justo, F. de Brito Mota, A. Fazzio, Phys. Rev. B 65 (2002) 73202.
[133] L. Martin-Moreno, E. Martinez, J. Verges, F. Yndurain, Phys. Rev. B 35 (1987) 9683.
[134] W. Warren, F. Rong, E. Poindexter, G. Gerardi, J. Kanicki, J. Appl. Phys. 70 (1991) 346.
[135] W. Warren, J. Kanicki, J. Robertson, P. Lenahan, Appl. Phys. Lett. 59 (1991) 1699.
[136] P. Lenahan, S. Curry, Appl. Phys. Lett. 56 (1990) 157.
[137] T. Makino, M. Maeda, Jpn. J. Appl. Phys. 25 (1986) 1300.
[138] A. Iqbal, W. Jackson, C. Tsai, J. Allen, C. Bates, J. Appl. Phys. 61 (1987) 2947.
[139] R. Karcher, L. Ley, R. Johnson, Phys. Rev. B 30 (1984) 1896.
[140] J. Robertson, Philos. Mag. B 66 (1992) 615.
[141] A. Morimoto, T. Miura, M. Kumeda, T. Shimizu, Jpn. J. Appl. Phys. 21 (1982) L119.
[142] R. Konenkamp, Phys. Rev. B 36 (1987) 2938.
[143] E. Kalabukhova, S. Lukin, D. Savchenko, B. Shanina, A. Vasin, V. Lysenko, A. Nazarov, A. Rusavsky, J. Hoentsch, Y. Koshka, Phys. Rev. B 81 (2010) 15539.
[144] F. Demichelis, F. Giorgis, C. Pirri, E. Tresso, G. Amato, U. Coscia, Physica B 205 (1995) 169.
[145] A. Lowe, M. Powell, S. Elliott, J. Appl. Phys. 59 (1986) 1251.
[146] S. Habermehl, C. Carmignani, Appl. Phys. Lett. 80 (2002) 261.
[147] M. Maeda, Y. Arita, J. Appl. Phys. 53 (1982) 6852.
[148] B. Bittel, T. Pomorski, P. Lenahan, S. King, ECS Trans. 35 (2011) 747.
[149] A. Urbanowicz, K. Vanstreels, P. Verdonck, D. Shamiryan, S. De Gendt, M. Baklanov, J. Appl. Phys. 107 (2010) 104122.
[150] L. Zhao, Y. Barbarin, K. Croes, M. Baklanov, P. Verdonck, Z. Tokei, C. Claeys, Appl. Phys. Lett. 106 (2015) 072902.
[151] S. King, ECS J. Solid State Sci. Technol. 4 (2015) N3029.
[152] C. Chiang, I. Ko, M. Chen, Z. Wu, Y. Lu, S. Jang, M. Liang, J. Electrochem. Soc. 151 (2004) G93.
[153] Y. Uchida, S. Hishiya, N. Fujii, K. Kohmura, T. Nakayama, H. Tanaka, T. Kikkawa, Microelectron. Eng. 83 (2006) 2126.
[154] Y. Li, I. Ciofi, L. Carbonell, N. Heylen, J. Van Aelst, M. Baklanov, G. Groeseneken, K. Maex, Z. Tokei, J. Appl. Phys. 104 (2008) 034112.
[155] Y. Cheng, K. Leon, J. Huang, W. Chang, Y. Chang, J. Leu, Microelectron. Eng. 114 (2014) 12.
[156] C. Kubasch, H. Ruelke, U. Mayer, J. Bartha, ECS J. Solid State Sci. Technol. 4 (2015) N3118.
[157] T. Tan, C. Gan, A. Du, C. Cheng, J. Appl. Phys. 106 (2009) 043517.
[158] M. He, Y. Ou, P. Wang, T. Lu, Appl. Phys. Lett. 96 (2010) 222901.
[159] H. Miyazaki, D. Kodama, N. Suzumura, J. Appl. Phys. 106 (2009) 104103.
[160] L. Chen, W. Bang, Y. Park, E. Ryan, S. King, C. Kim, Appl. Phys. Lett. 96 (2010) 091903.
[161] J. Borja, J. Plawsky, T. Lu, W. Gill, T. Shaw, R. Laibowitz, E. Liniger, S. Cohen, R. Rosenberg, G. Bonilla, J. Vac. Sci. Technol. A 32 (2014) 051508.
[162] R. Achanta, J. Plawsky, W. Gill, Appl. Phys. Lett. 91 (2007) 234106.