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Al_2O_3 Insertion Layer for Improved PEALD SiO_2/(Al)GaN Interfaces

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The development of high-quality gate dielectric/III-N semiconductor interfaces is indispensable to achieve high performance GaN-based high electron mobility transistors (HEMTs). In this work, we present improved interfaces between SiO_2 and GaN (or AlGaN) with Al_2O_3 insertion layer deposited by plasma-enhanced atomic layer deposition (PEALD). Interface state density (D_{it}) and border trap density (N_{bt}) were characterized using UV-assisted C–V measurement on metal-oxide-semiconductor capacitors (MOSCAPs). SiO_2 with Al_2O_3 insertion layer exhibited integrated D_{it} of $1.93 \times 10^{11}\,cm^{-2}$, one order of magnitude lower than that without Al_2O_3 insertion layer. N_{bt} of SiO_2 with Al_2O_3 insertion layer is nearly twice of that without Al_2O_3 insertion layer. Stressed C–V measurement further confirmed improved interface with Al_2O_3 insertion layer. To investigate the performance of MOS-HEMT using SiO_2 with Al_2O_3 insertion layer as a gate dielectric, pulsed I_{DS}–V_{GS} measurements were performed. MOS-HEMT exhibited positive threshold voltage shift, which is attributed to electron trapping in interface states and border traps.

1. Introduction

GaN based high electron mobility transistors (HEMTs) are of particular interest for high-power switching applications owing to their superior physical properties such as high breakdown field and high electron mobility.[1,2] Metal-oxide-semiconductor (MOS) structures are preferred over conventional Schottky gates since they provide suppression of gate leakage, large operating voltage and the ability to achieve normally off operation.[3,4] However, deposition of foreign dielectrics on GaN results in the formation of a high-density of interface states ($D_{it} \approx 10^{12}-10^{13}\,eV^{-1}\,cm^{-2}$)[5] due to incomplete chemical bonds, structural damage and impurities at the dielectric/GaN interface. The interface states with both short and long emission time constants, are in electrical communication with the underlying semiconductor. Interface states can be charged and discharged depending on the surface potential and thus result in the threshold voltage instability of MOS-HEMTs.[6–8] Therefore, the development of high-quality gate dielectric/III-N interfaces plays perhaps the most significant role in achievement of high performance MOS-HEMTs.

Various oxide materials have been reported as gate dielectric for GaN MOS-HEMTs. For example, Si_3N_4 deposited by in situ metalorganic chemical vapor deposition (MOCVD),[9] Al_2O_3 deposited by MOCVD[10] or atomic layer deposition (ALD),[11–13] HfO_2 deposited by ALD[14,15] and SiO_2 deposited by ALD[16] or plasma enhanced chemical vapor deposition.[17] Among these, Al_2O_3 and SiO_2 have been two of the most suitable oxides owing to their relatively large conduction band offset (CBO) with GaN and large breakdown electric field. However, the CBO of Al_2O_3 ($\approx$2.13 eV)[18] is smaller than that of SiO_2 ($\approx$3.6 eV),[19] resulting in considerable gate leakage current. On the other hand, the interface state density (D_{it}) of SiO_2/GaN is larger than Al_2O_3/GaN, resulting in a severe threshold voltage instability. Composite gate dielectric has been proposed to overcome the disadvantage given by a single dielectric. For example, Kambayashi et al.[20] showed a gate stack consisting of ALD Al_2O_3 and MW-PECVD SiO_2 with high breakdown field and low interface state density. Kikuta et al.[21] reported Al_2O_3/SiO_2 nanolaminate with different ratio of Al_2O_3 to SiO_2 for a gate dielectric in GaN-based transistors.

In this paper, improved interfaces between plasma enhanced ALD (PEALD) SiO_2 and GaN (or AlGaN) are demonstrated, with an Al_2O_3 insertion layer. D_{it} and N_{bt} were characterized using UV-assisted C-V measurement on MOSCAPs. Pulsed I_{DS}-V_{GS} measurements were performed on MOS-HEMT to evaluate threshold voltage shifts related to interface states with long emission times and border traps.

2. Experimental Section

2.1. MOSCAP

The GaN epilayer was grown on 2-inch diameter sapphire substrate by MOCVD. The layer structure, shown in **Figure 1**(a)

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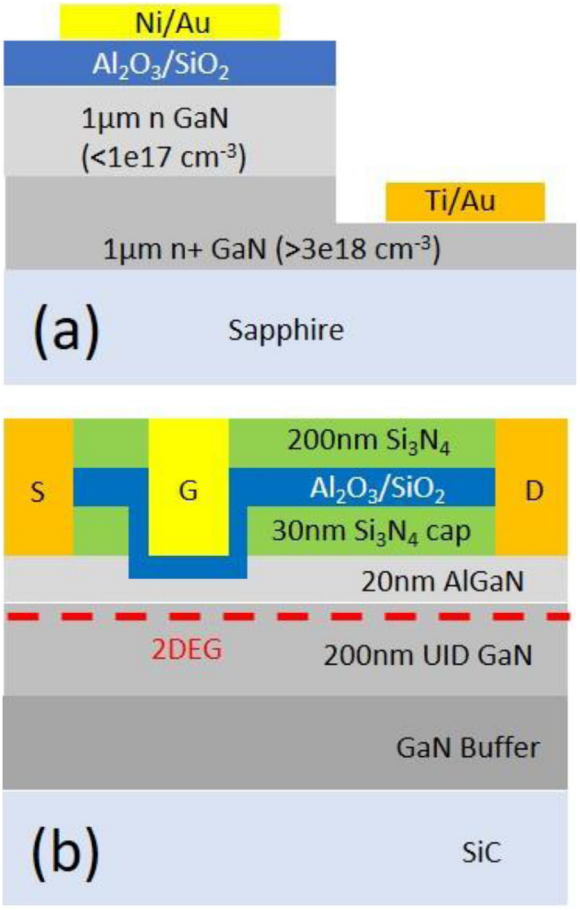

Figure 1. Schematic diagram of (a) PEALD Al_2O_3/SiO_2 MOSCAP and (b) AlGaN/GaN MOS-HEMT.

consists of 1 μm n^+ GaN with doping of $\approx 3 \times 10^{18}\,cm^{-3}$ and 1 μm n GaN with doping of $\approx 1 \times 10^{17}\,cm^{-3}$. Following a standard solvent clean of the sample, in situ N_2/H_2 plasma pretreatment in the PEALD chamber was carried out prior to the dielectric deposition. The sample was annealed at 400 °C in N_2 ambient for 15 min after the plasma pretreatment to alleviate the surface damage. Twenty cycles of Al_2O_3 deposition was performed using dimethylaluminum isopropoxide (DMAI) and O_2 as precursors, followed by 200 cycles of SiO_2 deposition using tris(dimethylamino)silane (TDMAS) and O_2 plasma as precursors at room temperature. The thickness of Al_2O_3 and SiO_2 was determined to be ≈2 and 20 nm respectively, from the product of the number of deposition cycles and the foreknown deposition rate which were 1.1 and 1.0 Å/cycle for Al_2O_3 and SiO_2 respectively. In situ X-ray photoelectron spectroscopy (XPS) analysis was conducted after the deposition of the insertion and bulk layers. The sample was annealed, post-deposition, in N_2 ambient at 400 °C for 15 min. MOSCAP shown in Figure 1 with diameter of 200 μm was fabricated with the following steps. Mesa isolation consisted of CHF_3/Ar (25 sccm/25 sccm) RIE to etch SiO_2 and BCl_3/Cl_2/Ar (8 sccm/30 sccm/5 sccm) ICP to etch GaN. Then, gate contacts consisting of Ni/Au (20 nm/200 nm) were formed on the oxides by e-beam evaporation and lift-off process. Finally, Ohmic contacts consisting of Ti/Au (20 nm/200 nm) were formed on the n^+ GaN. The SiO_2/GaN MOSCAP without Al_2O_3 insertion layer was prepared for comparison. The thickness of SiO_2 was 22 nm to maintain the same physical oxide thickness with the MOSCAP with Al_2O_3 insertion layer.

2.2. MOS-HEMT

The device schematic of the AlGaN/GaN MOS-HEMT is depicted in Figure 1. MOCVD grown AlGaN/GaN HEMT structures consisted of 30 nm Si_3N_4 cap layer, 20 nm $Al_{0.25}Ga_{0.75}N$, 200 nm UID GaN, and Fe-doped GaN buffer layer on SiC substrate. Mesa isolation was performed by CHF_3/O_2 RIE to etch Si_3N_4 and BCl_3/Cl_2 ICP to etch AlGaN/GaN. Source/drain Ohmic contacts consisting of Ti/Al/Ni/Au were formed by e-beam deposition and a lift-off process on the AlGaN layer, which was then annealed at 860 °C for 30 s in an N_2 ambient. PEALD SiO_2 with Al_2O_3 insertion layer were then deposited as gate dielectric. Gate contacts consisting of Ni/Au/Ni were defined using a lift-off process. 200 nm PECVD Si_3N_4 was deposited as a passivation layer. Finally, source, drain and gate vias were formed. The fabricated MOS-HEMT features a gate length of 1 μm, a gate to source distance of 2 μm and a gate to drain distance of 6 μm. The gate width is 50 μm.

3. Physical Characterization

Figure 2 shows the combined element profile of the insertion oxide layer and bulk oxide layer analyzed by XPS. Al 2p core-level spectrum was determined near the interface and Si 2s core-level spectrum was determined in the bulk. It indicates that the oxide consists of Al_2O_3 insertion layer and SiO_2 bulk layer.

4. Electrical Characterization

4.1. Forward I–V Measurement

Breakdown field (E_{br}) was characterized by forward-biased I–V measurements on MOSCAPs using a Keithley 4200-SCS parameter analyser with a sweep rate of 0.56 $V\,s^{-1}$. The electric

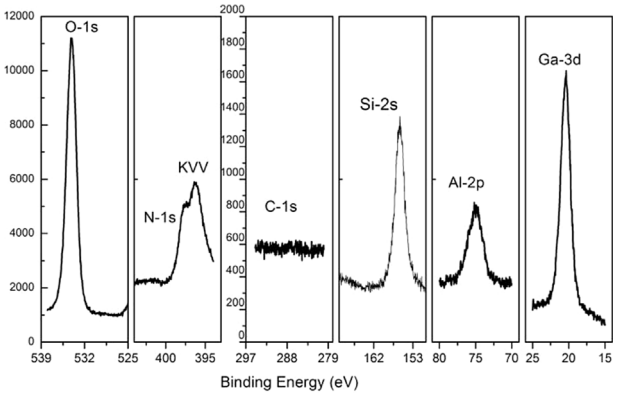

Figure 2. Element profile of the oxide thin film on GaN analyzed by XPS.

field across the oxide is determined by the gate voltage over the equivalent oxide thickness (E_{OT}) in terms of SiO_2. E_{OT} can be calculated using the following equation: $E_{OT} = t_{SiO2} + t_{Al2O3}\frac{k_{SiO2}}{k_{Al2O3}}$. **Figure 3** shows current density-electric field characteristics of MOSCAP with and without Al_2O_3 insertion layer. The E_{br} of MOSCAP with Al_2O_3 insertion layer (8.5 MV cm^{-1}) is slightly higher than that of MOSCAP without Al_2O_3 insertion layer (8.0 MV cm^{-1}) because E_{OT} for MOSCAP with Al_2O_3 insertion layer, 20.88 nm is slightly lower than that for MOSCAP without Al_2O_3 insertion layer, 22 nm.

4.2. UV-assisted C–V Measurement

D_{it} was characterized using UV-assisted C–V measurement,[22] with a modified Terman method for wide bandgap semiconductors. Although the conductance method has been widely used to evaluate the interface state density,[23,24] it can only measure interface states with short emission times and hence underestimates the interface state density in GaN devices due to the lack of hole generation. UV-assisted C–V measurements based on UV illumination to generate electron-hole pairs is preferred as the method gives more accurate detail of the interface state density as a function of energy. C–V characteristics were measured using a Keithley 4200-SCS parameter analyser at 1 MHz frequency, 80 mV s^{-1} sweep rate and 30 mV amplitude AC signal. An OmniCure 1500 spot curing system with UV intensity peaks at 365, 400, and 430 nm wavelength was used as the UV illumination source. The energy of 365 nm UV is equivalent to ≈3.41 eV, corresponding to the GaN bandgap. **Figure 4** shows UV-assisted C–V measurement data for the MOSCAP. First, the MOSCAP was held in accumulation for 10 min to eliminate the initial variation in occupancy of interface states. Then a dark C–V curve was obtained by sweeping the MOSCAP from depletion to accumulation under the dark condition. Next, the MOSCAP was exposed to UV in depletion for 30 s to neutralize the filled interface states. It was then held in depletion for an additional 10 min after turning off the UV to let free holes leave the MOSCAP. Finally, post-UV curve was obtained by sweeping the device from depletion to accumulation under dark condition. A reference curve was obtained by overlapping the depletion portion of the dark curve to that of the post-UV curve.

The voltage difference between the post-UV curve and reference curve (ΔV) at a given capacitance, determines the trapped interface states (the states that exist above the Fermi level). The change in ΔV thus corresponds to the change in the occupancy of interface states due to the change in Fermi level. The position of the Fermi level is related to the surface potential (ψ_s). Hence, D_{it} as a function of energy level can be determined by

$$D_{it} = \frac{C_{ox}}{q}\frac{d\Delta V}{d\Psi_s} \quad (1)$$

where C_{ox} is the oxide capacitance.

The flatband voltage shift (ΔV_{FB}) is associated with traps that are disconnected from the Fermi level since the existence of depletion region prevents bulk electrons in GaN from being trapped. These traps can only be occupied when the MOSCAP is in accumulation. These traps are located near the interface within the oxide, usually called border traps.[25] The amount of

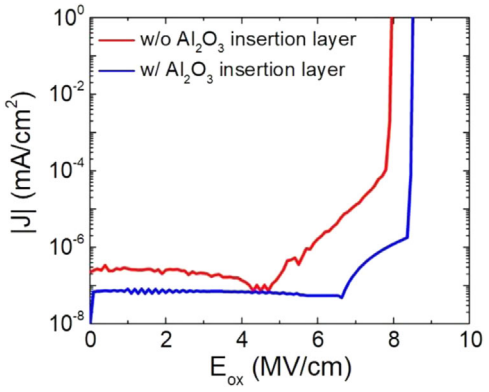

Figure 3. Current density-electric field characteristics of 200 μm diameter MOSCAP with and without Al_2O_3 insertion layer.

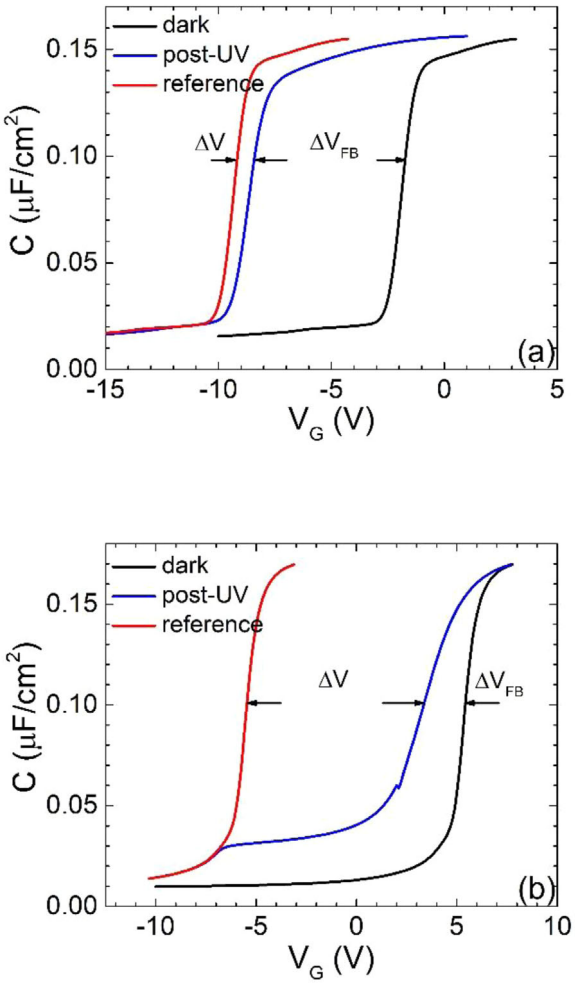

Figure 4. UV-assisted C–V measurement data for SiO_2/GaN MOSCAP (a) w/ Al_2O_3 insertion layer and (b) w/o Al_2O_3 insertion layer.

border traps (N_{bt}) can be obtained by

$$N_{bt} = \frac{C_{ox}\Delta V_{FB}}{q} \quad (2)$$

Figure 5 plots D_{it} of SiO_2 with and without the Al_2O_3 insertion layer as a function of energy level calculated from Eq. (1). There is a peak in the D_{it} curve for SiO_2 without Al_2O_3 insertion layer. Yeluri et al.[26] pointed out that the peak is attributed to the holes at the interface, in the case of material like SiO_2 with a positive valence band offset to GaN (≈2 eV).[19] The valence band barrier at the interface prevents holes from leaving the system, affecting the measurement. The contribution of holes to the measurement corresponds to the shadow area under the peak as shown in Figure 5. On the other hand, there is no peak in the D_{it} curve for SiO_2 with an Al_2O_3 insertion layer. A possible explanation is that the Al_2O_3 insertion layer assists holes with tunneling through the valence band barrier. When the MOSCAP is under negative bias condition, holes first direct tunnel (DT) through Al_2O_3 insertion layer and subsequently reach the valence band of SiO_2 by trap-assisted tunneling (TAT). Such combination of DT and TAT mechanism was reported by Bhuyian et al. for a high-k dielectric with an interfacial layer.[27]

SiO_2 with Al_2O_3 insertion layer has much lower D_{it} than SiO_2 without Al_2O_3 insertion layer near the conduction band. **Table 1** lists D_{it} integrated from E_c–E = 0.15 eV to E_c–E = 1 eV. The integrated D_{it} for SiO_2 with and without Al_2O_3 insertion layer are 1.93×10^{11} and $3.83 \times 10^{12}\,cm^{-2}$ respectively. D_{it} decreased by one order of magnitude with the presence of an Al_2O_3 insertion layer. The values of N_{bt} calculated from Eq. (2) are summarized in Table 1. N_{bt} of SiO_2 with Al_2O_3 insertion layer is nearly twice that of SiO_2 without Al_2O_3 insertion layer.

4.3. Stressed C-V Measurement

The MOSCAP was swept from depletion to accumulation, followed by the constant DC bias stress (4 V). After the stress, the accumulation to depletion curve was recorded for changes in the flatband voltage (ΔV_{FB}) with respect to the virgin depletion to accumulation curve. The same procedure was repeated for different stress period. **Figure 6** plots ΔV_{FB} as a function of stress period for SiO_2 with and without Al_2O_3 insertion layer. ΔV_{FB} is a measure of total net added charge (N_{total}) during the stress. ΔV_{FB} for SiO_2 without Al_2O_3 insertion layer increases significantly with the increase of stress period. Corresponding N_{total} is $\approx 3.0 \times 10^{12}\,cm^{-2}$ when stress period is 1000 s. On the other hand, ΔV_{FB} for SiO_2 with Al_2O_3 insertion layer is independent on stress period. Corresponding N_{total} is $\approx 1.0 \times 10^{11}\,cm^{-2}$. The value of N_{total} is very closed to D_{it} for both dielectrics, implying that total net added charge is dominated by charging of interface states. Stressed C–V measurement also reveals that improved interface is obtained with Al_2O_3 insertion layer.

Table 1. Dit and Nbt of SiO_2 with and without Al_2O_3 insertion layer.

SiO_2	Integrated D_{it} over 0.15 to 1 eV (cm^{-2})	N_{bt} (cm^{-2})
w/o Al_2O_3	3.83×10^{12}	3.39×10^{12}
w/Al_2O_3	1.93×10^{11}	6.63×10^{12}

4.4. Pulsed I_{DS}-V_{GS} Measurement

While D_{it} and N_{bt} can be quickly obtained by analysing the MOSCAP, it does not provide a direct indication of the effect on the performance of an actual MOS-HEMT. Pulsed I_{DS}-V_{GS} measurements have been used for interface state and border traps analysis in AlGaN/GaN MOS-HEMT.[28,29] In this work, the same method was conducted on AlGaN/GaN MOS-HEMT shown in Figure 1. The measurement features a constant drain bias (V_{DS} = 10 V) and a set of pulsed gate bias consisting of both low-base up-sweep and high-base down-sweep. The up-sweep and down-sweep waveforms applied at the gate are shown in **Figure 7**. The pulse width and pulse period are 5 μs and 100 ms. In the up-sweep measurements, the base voltage (V_{base}) is held at −10 V, much lower than V_t, to avoid electrons spill-over.[24] The pulse amplitude was gradually increased from V_{base} to maximum gate bias ($V_{GS,max}$ = 10 V) in steps of 0.1 V. The interface states are intended to be empty during the up-sweep measurements since the electron trapping is minimized by

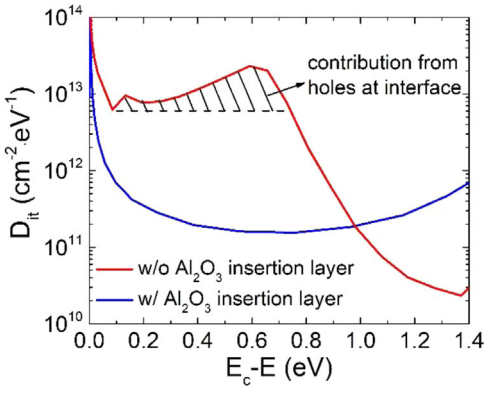

Figure 5. D_{it} as a function of energy level.

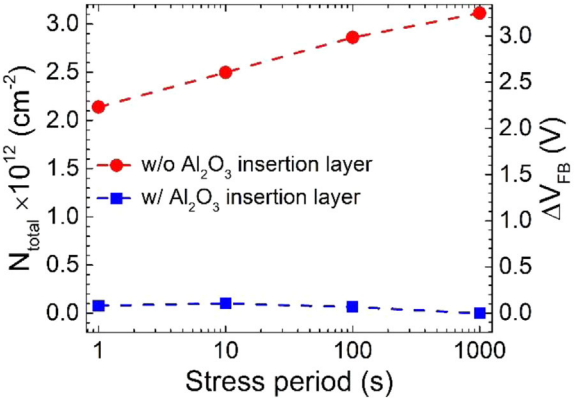

Figure 6. N_{total} and ΔV_{FB} as a function of stress period.

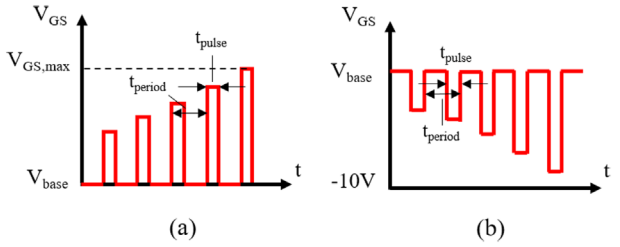

Figure 7. Waveform of V_{GS} during pulsed I_{DS}-V_{GS} measurement: (a) low-base up-sweep and (b) high-base down-sweep.

short pulse and long period. In the down-sweep measurements, V_{base} is held at high voltage, from 3 to 10 V. The pulse height is gradually decreased from V_{base} to −10V in steps of −0.1 V. The interface states below the Fermi level with emission time constant longer than the pulse width are filled in the down-sweep measurements. A certain amount of border traps is inevitably filled by electron spill-over in the meantime. Therefore, the threshold voltage difference between up-sweep and down-sweep (ΔV_t) is attributed to the interface states with emission time constants longer than the pulse width as well as border traps.

The corresponding total traps (N_{total}) can be calculated by

$$N_{\text{total}} = N_{bt} + D_{it} = \frac{C_{ox}\Delta V_t}{q} \tag{3}$$

Figure 8 shows pulsed I_{DS}-V_{GS} characteristics of AlGaN/GaN MOS-HEMT. **Figure 9** plots N_{total} and ΔV_t versus V_{base} of the down-sweep calculated from Eq. (3). Increasing ΔV_t is due to the increasing amount of electron trapping in interface states and border traps as V_{base} increases. It should be noted that the pulsed I_{DS}-V_{GS} measurement neither maps D_{it} as a function of energy level nor distinguishes interface states from border traps, unlike the UV-assisted C-V measurement. It evaluates the threshold voltage shift related to the combination of interface states and border traps within a certain detectable energy range, which is given by Shockley-Read-Hall statistics

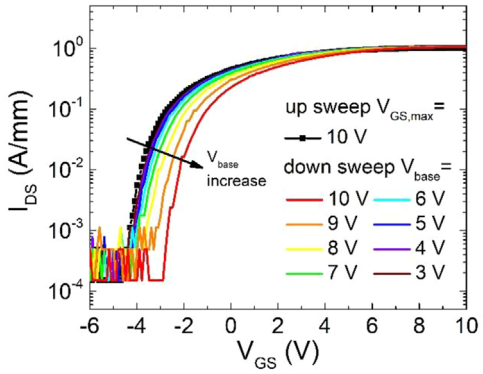

Figure 8. Pulsed I_{DS}-V_{GS} measurement on AlGaN/GaN MOS-HEMT.

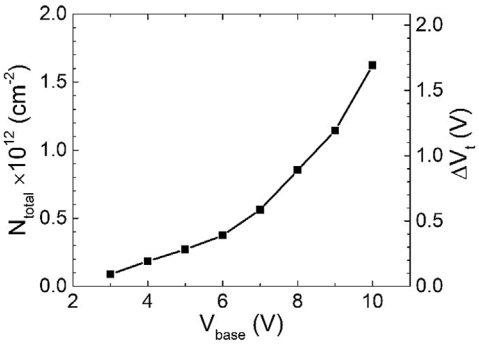

Figure 9. N_{total} versus V_{base} in the down-sweep measurement.

$$\tau = \frac{1}{v_{th}\sigma_n N_c}\exp\left(\frac{E - E_c}{kT}\right) \tag{4}$$

where v_{th}, σ_n and N_c are electron thermal velocity, electron capture cross section and density of states in the conduction band in GaN, respectively.[30] The detectable energy range is calculated to be E_c–$E \geq 0.38$ eV.

5. Conclusion

Improved interfaces between SiO_2 and GaN (or AlGaN) have been obtained with an Al_2O_3 insertion layer. XPS revealed that the oxide consists of an Al_2O_3 insertion layer near interface and SiO_2 in the bulk. Forward I–V measurement and UV-assisted C–V measurements were performed on PEALD SiO_2/GaN MOS-CAP to characterize the E_{br}, D_{it} and N_{bt}. D_{it} decreased by one order of magnitude with the insertion of Al_2O_3 layer. N_{bt} increased by 2×. Stressed C–V measurements also confirmed improved interface for SiO_2 with Al_2O_3 insertion layer. Pulsed I_{DS}–V_{GS} measurements were performed on AlGaN/GaN MOS-HEMTs to evaluate threshold voltage shifts related to interface states with long emission times and border traps. MOS-HEMTs exhibited positive ΔV_t, attributing to electron trapping in interface states and border traps.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

Al_2O_3, border traps, GaN, insertion layers, interface state density, SiO_2

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